SuperSpeed USB 3.1

Physical Layer Test Challenges and Solutions

Agenda

- ❑ Agilent Digital Standards Program
- ❑ USB Industry and Specification Updates
- ❑ USB-IF Test Labs
- ❑ USB 2.0/3.0 Compliance Update
- ❑ USB 3.1 Transmitter Testing
- ❑ USB 3.1 Receiver Testing
- ❑ Cable/Connector Testing
- ❑ Summary
- ❑ Questions

Agilent Digital Standards Program

- Our solutions are driven and supported by Agilent experts
  involved in international standards committees:
  - Joint Electronic Devices Engineering Council (JEDEC)
  - PCI Special Interest Group (PCI-SIG®)
  - Video Electronics Standards Association (VESA)
  - Serial ATA International Organization (SATA-IO)
  - USB-Implementers Forum (USB-IF)
  - Mobile Industry Processor Interface (MIPI) Alliance
  - And many others
- We're active in standards meetings, workshops, plugfests, and seminars
  .
- We get involved so you benefit with the right solutions when you need them

We understand your future requirements, because we help shape them

Rick Eads
PCI-Sig Board Member

Brian Fetz
DisplayPort Phy CTS Editor
VESA Board Member

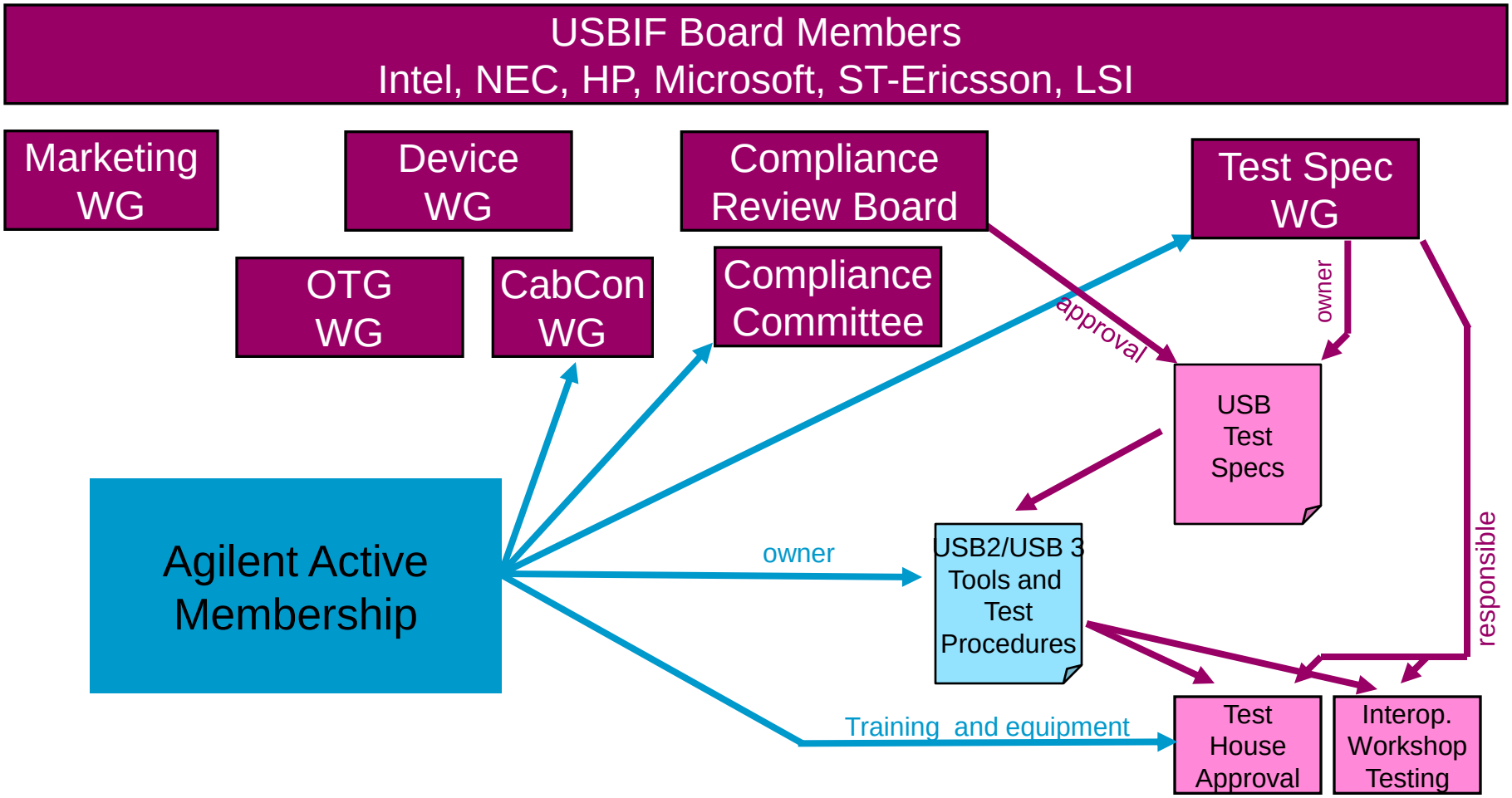
Jim Choate
USB-IF Compliance Committee
USB 3.0 Electrical Test Spec WG

Min-Jie Chong
SATA 6G / PHY / LOGO Contributor
SATA-IO Gold Suite Lead

Perry Keller
JEDEC Board Member

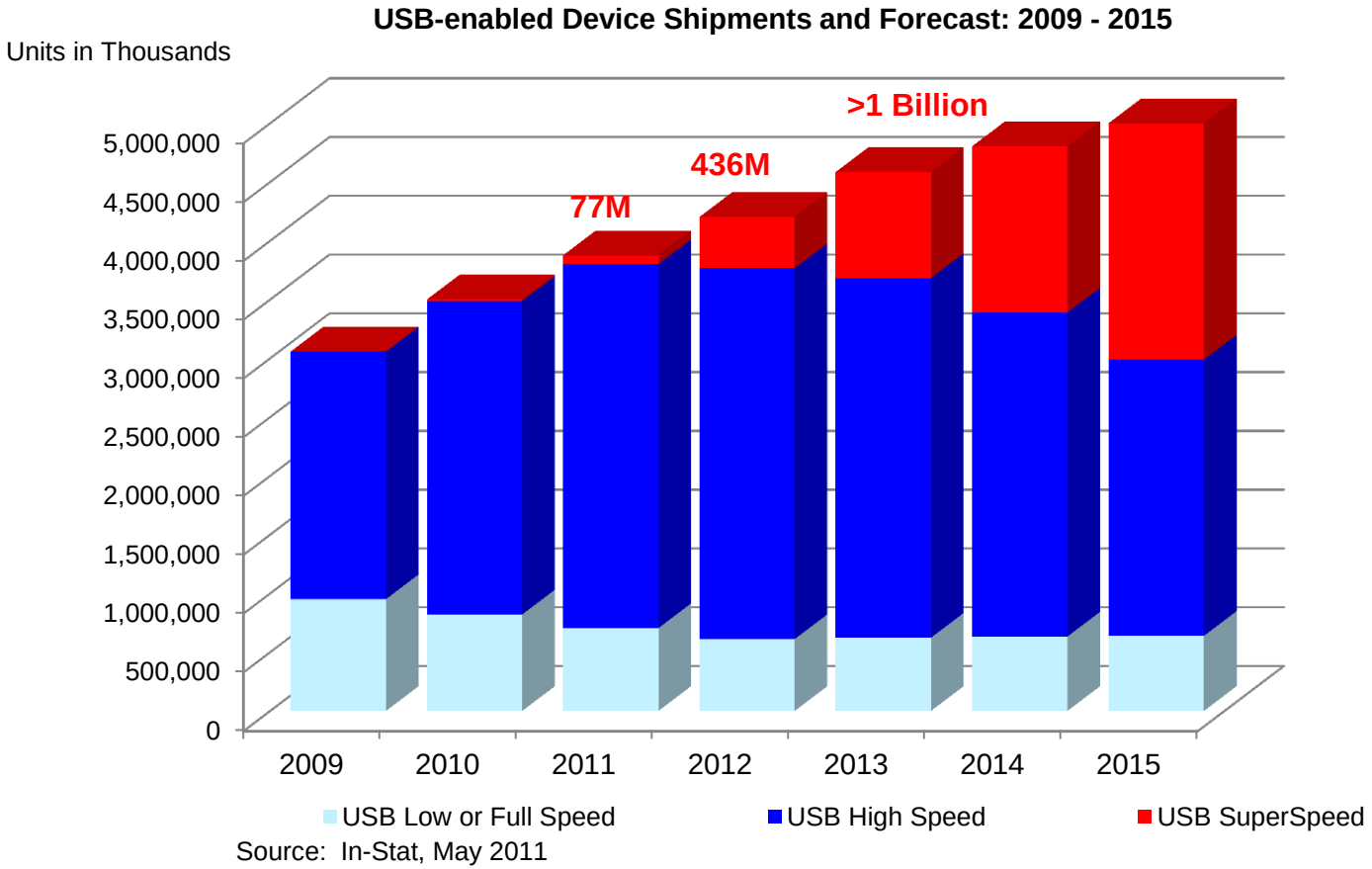
The Agilent Infiniium Scopes team maintains engagement in the top high tech standards organizations

USB Implementers Forum, inc (USB-IF)



Worldwide Shipment of USB-enabled Devices

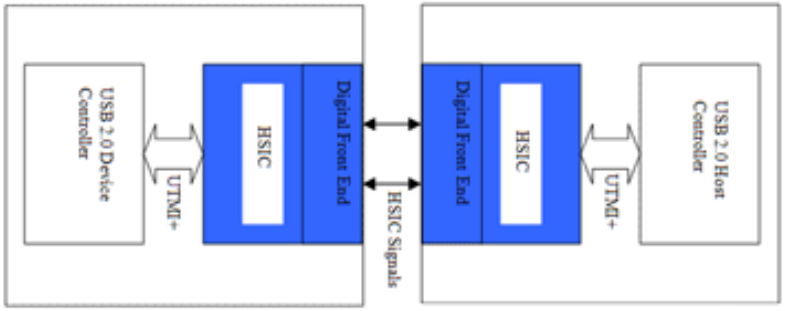
- USB is the most successful interface in the history of PC
- Device charging over USB has become a major consumer feature
- USB installed base is 10+ billion units and growing at 3+ billion units a year
- Adoption is virtually 100% in PC and peripheral categories



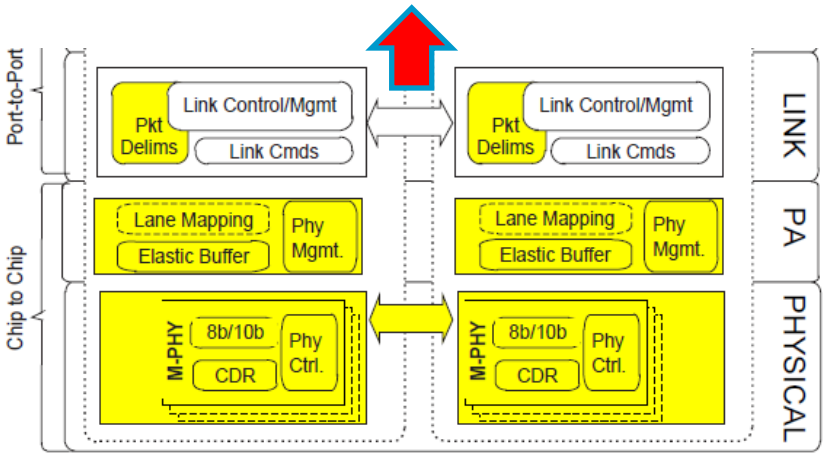
Source: In-Stat, May 2011

USB-IF Specification updates and additions

- HSIC – a low power USB chip to chip solution designed for mobile applications
- SSIC – USB 3.0 performance extension for chip to chip solution designed for mobile applications (download with USB 3.0 spec). Uses M-PHY for physical layer.
- USB Power Delivery Spec– an expansion of USB power delivery to allow more flexible power delivery up to 100W. Power direction is no longer fixed. http://www.usb.org/developers/powerdelivery/
- Battery Charging Specification 1.2
- All USB-IF specifications are available at http://www.usb.org/developers/docs/



USB 3.0 SuperSpeed above Link Layer



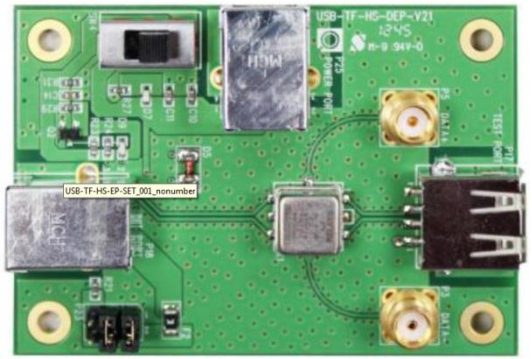
Key Features of USB Power Delivery Spec

- Increases negotiated power up to 100W
- Sink/source can be swapped, power direction no longer fixed
- Communication of PD device capabilities occurs over Vbus and optionally over USB.

USB 2.0 and 3.0 Updates

USB 2.0 Updates

- Testing requirements evolve over time:
- Details can be found at
- http://compliance.usb.org/index.html
- Rise/Fall time measurement
- High Speed SQ testing fixture change – direct SMA cable to scope
- High Speed test J and K testing



USB 3.0 Updates

- Current testing reference equalizer is for a long channel
- 3m cable plus long host PCB trace (~18-20dB differential insertion loss).
- ECN 18 – radio friendly SSC
- ECN - short channel equalizer

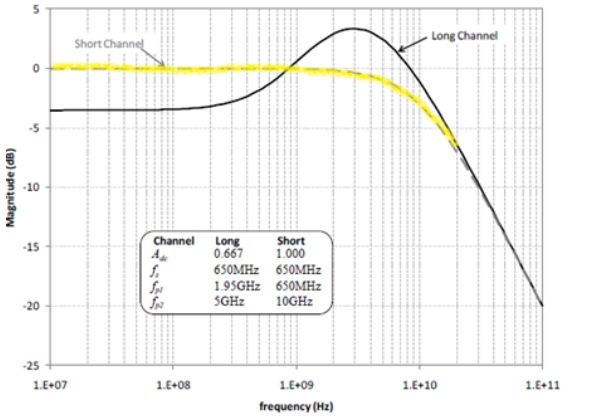
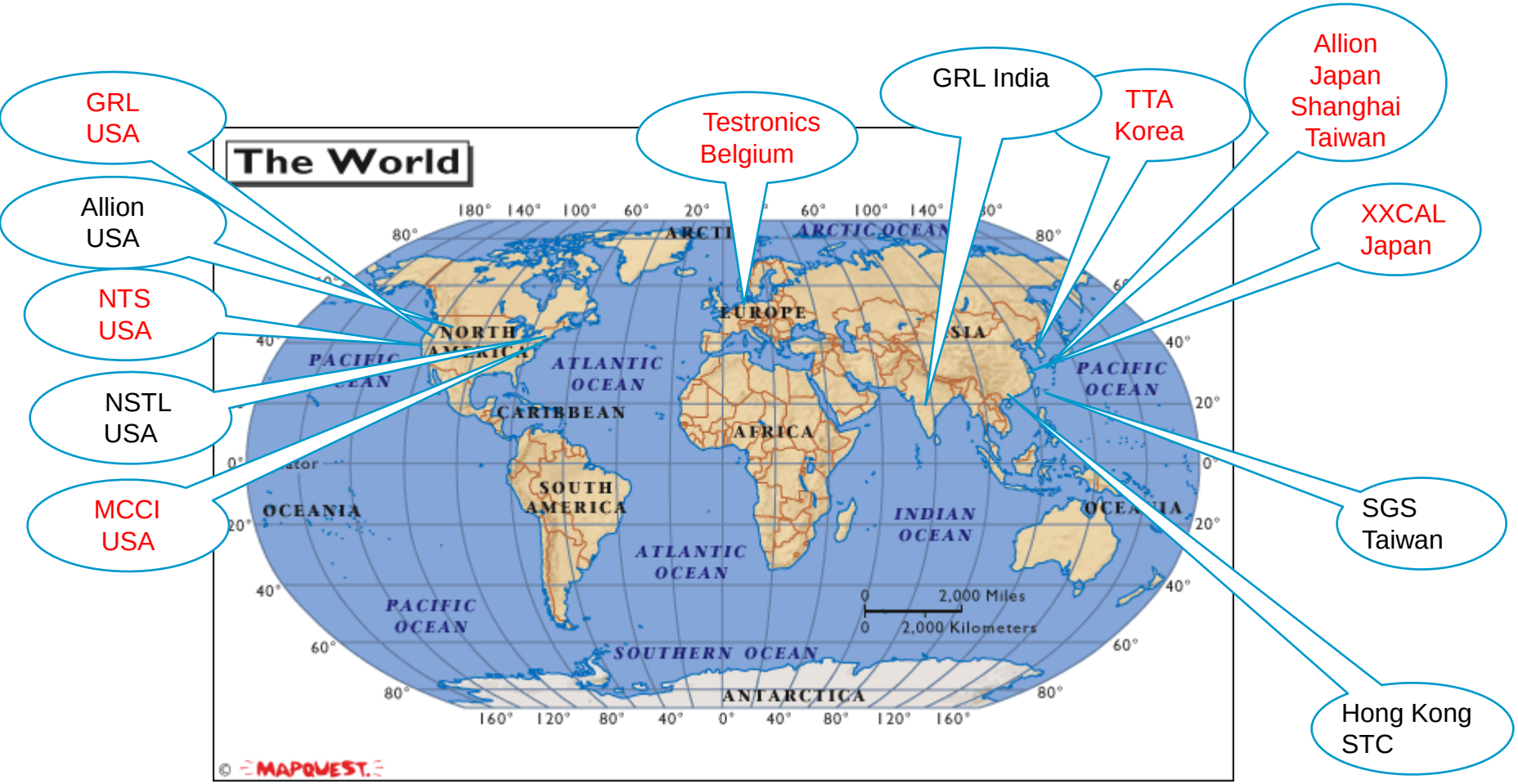


Figure 6-17. Tx Compliance Rx EQ Transfer Functions

Agilent is the USB2 and USB3 leading solution provider to test labs worldwide



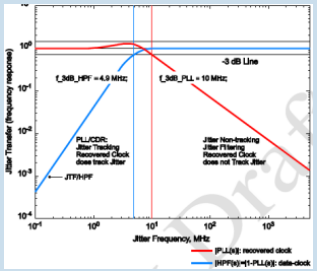
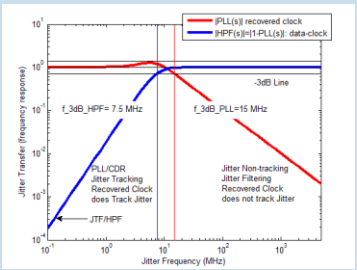
*Test Labs Currently Qualified for USB 3.0 Certification
Approved labs are listed at http://www.usb.org/developers/compliance/labs

Terminology – Specification Chapter 2

Here are some terms and their meanings used during this presentation

- Gen1 – Superspeed USB 3.0 5Gbps signaling rate
- Gen2 – 10Gbps signaling rate
- GenX – Any of the above
- SuperSpeed – Gen1 PHY requirements (5Gbps)
- SuperSpeedPlus – Gen2 PHY requirements (10Gbps)

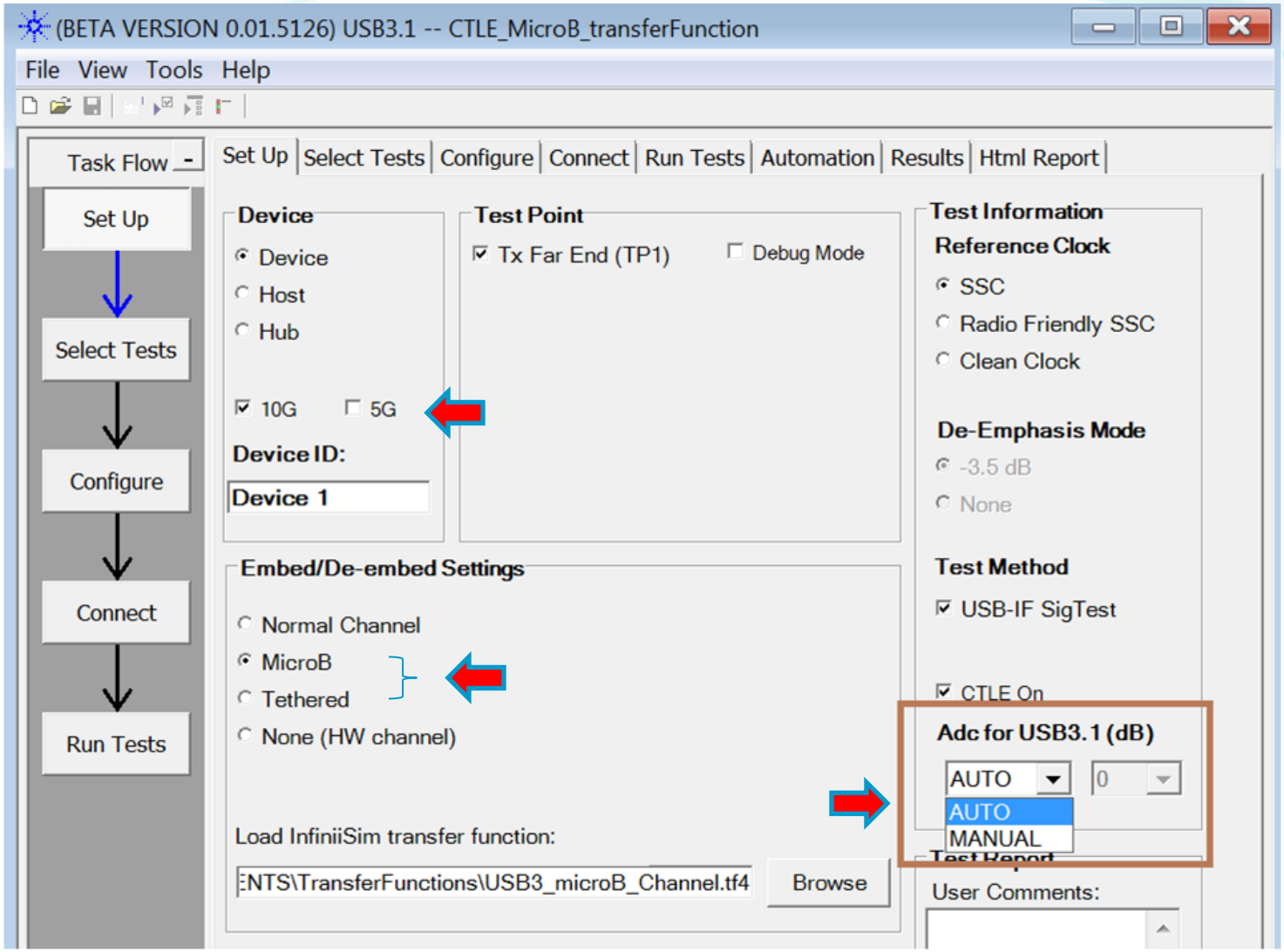
USB 3.1 gen1 vs. gen2 Overview

	Gen1	Gen2
Data rate	5Gb/s	10Gb/s
Coding	8b/10b	128b/132b scrambler: G(X) = X23 + X21 + X16 + X8 + X5 + X2 + 1
SKP	K28.1, K28.1	SKPOS with variable number of SKPs
LFPS	Training, warm reset or side band signaling protocol (pwr mgmt)	Device host capability negotiation is done during LFPS phase using LFPS modulation schemes
CDR	JTF BW 4.9Mhz 	JTF BW 7.5Mhz 
SSC	Slew rate test	New df/dt requirement: 1250 (max) ppm/µs
De-emphasis	Post: -3dB *Required*	Pre: 2.7dB Post: -3.3dB *Informative*
RX Ref EQ	CTLE	CTLE (6 level) + 1 tap DFE
Eye Height, TJ	100mV, 132ps (.66UI)	70mV, 71.4ps (.714UI)

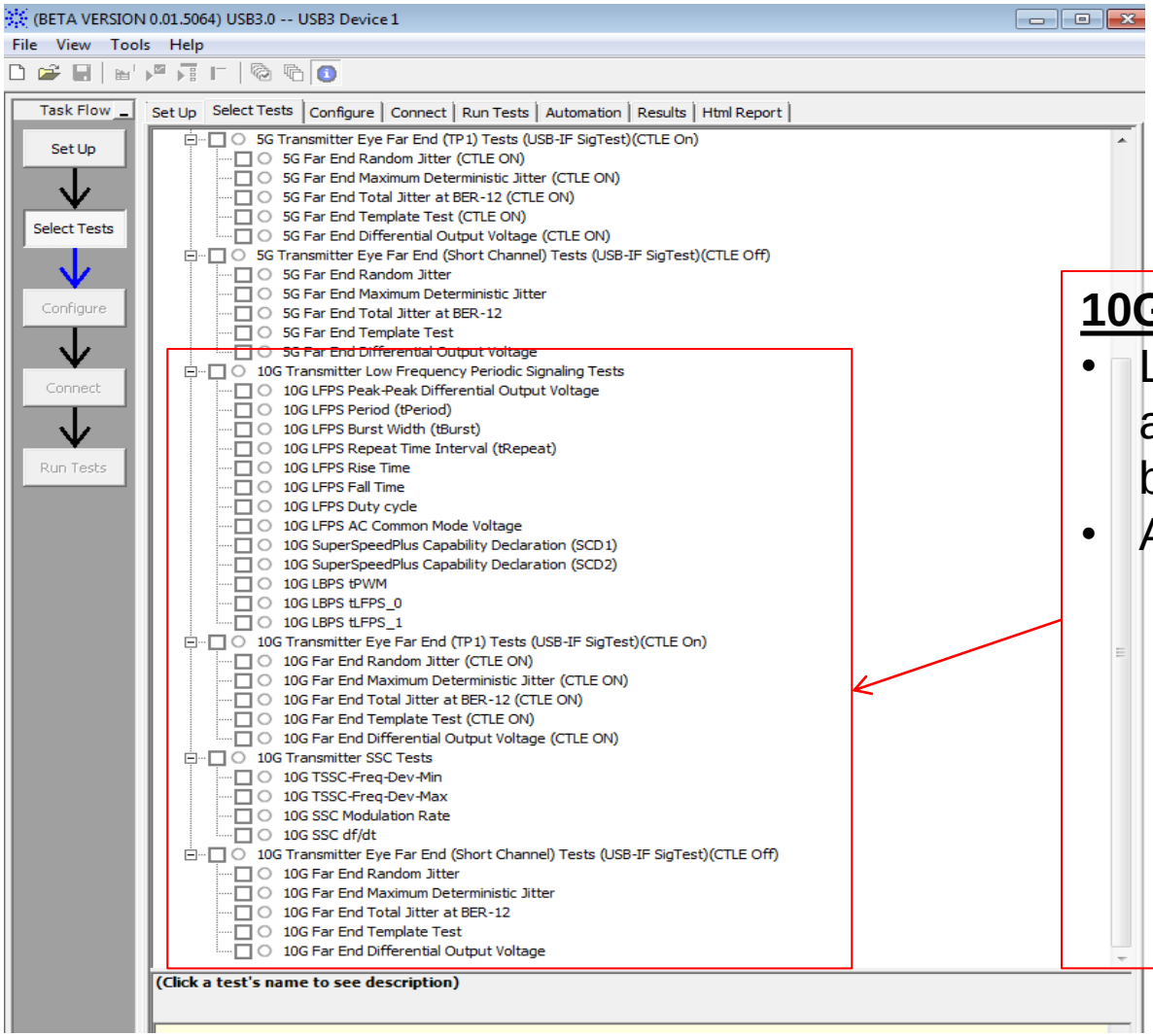
Transmitter Compliance Testing Overview

3.0	3.1	TP		
x	x	CP0	TX 5G Eye	Eye, Tj
	x	CP9	TX 10G Eye	Eye, Tj
x	x	CP1	SSC Mod Rate, UI and Deviation	ECN15, 18
	x	CP10	SSC Mod Rate, UI and Deviation	
x	x	CP1	Max Slew Rate	Rj
	x	CP10	SSC df/dt	Rj
x	x	LFPS	Vcm, Vdiff, rt/ft, DCycle, tPeriod, tBurst, tRepeat	
	x	LFPS	tPeriod-SSP, tRepeat-0, tRepeat-1, LPBM, tLFPS-0, tLFPS-1	
	X	TBD	Other test requirements may be identified during Test Specification development and early product testing	TBD

Agilent USB 3.1 TX Compliance Application



Agilent USB 3.1 TX Compliance Application

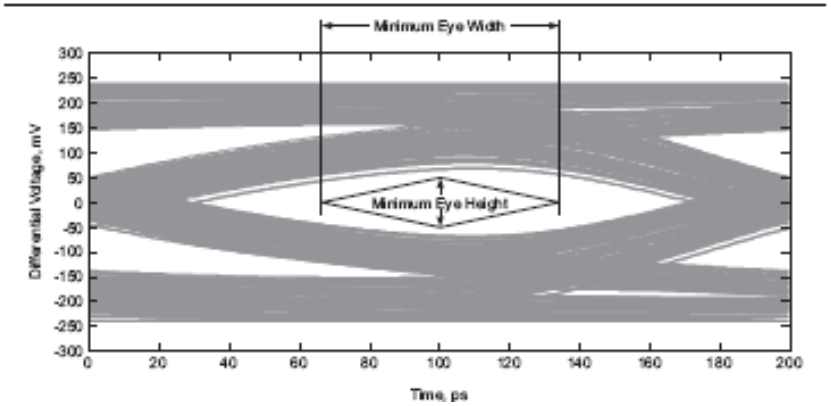


10G Test Requirements:

- Like 5G testing LFPS, SSC and SSC requirements must be checked
- Additional tests:
  - SCD1, SCD2
  - LBPS tPWM
    - tLFPS_0
    - tLFPS_1
  - SSC df/dt
  - Eye and Jitter after variable CTLE + DFE

Transmitter test requirements

The eye diagrams are to be measured into 50-Ω single-ended loads.



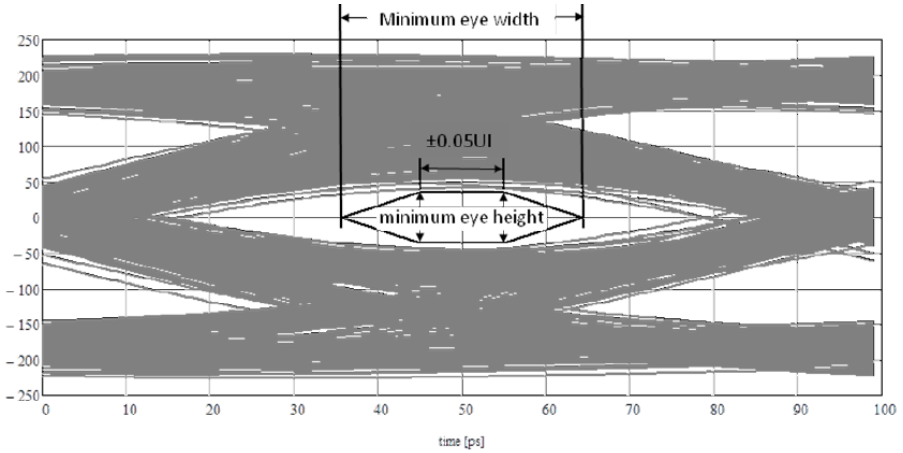
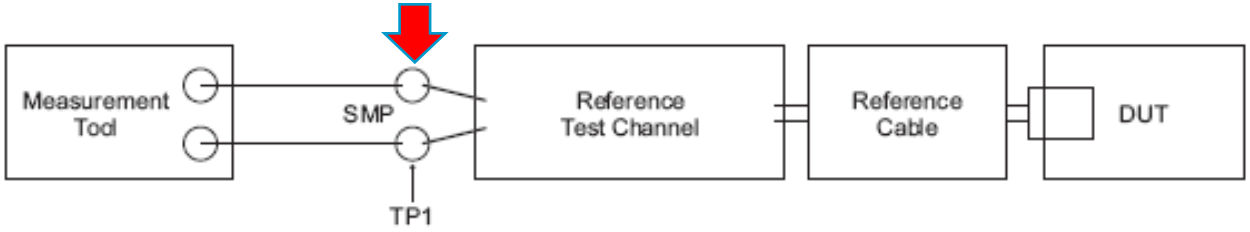


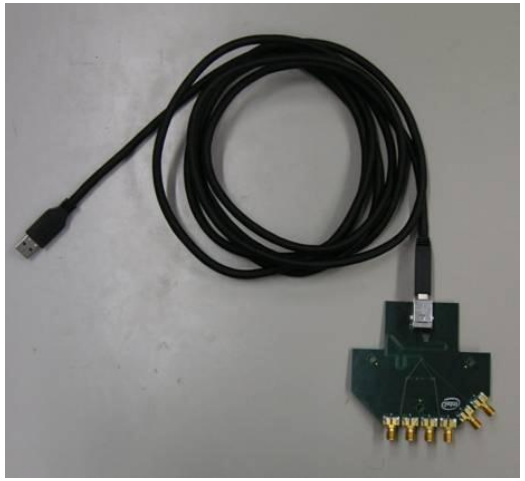
Table 6-19. Normative Transmitter Eye Mask at Test Point TP1

	5GT/s			10GT/s				
Signal Characteristic	**Minimum**	**Nominal**	**Maximum**	**Minimum**	**Nominal**	**Maximum**	**Units**	**Note**
Eye Height	100		1200	70		1200	mV	2,4
Dj			0.43			0.530	UI	1,2,3
Rj			0.23			0.184	UI	1,2,3,5
Tj			0.66			0.714	UI	1,2,3

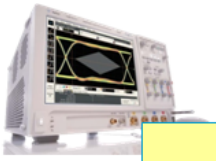
(TX Far End)



TX testing emulated through s-parameters



Embed Channel File
"DEVICE_3MCABLE.s4p"



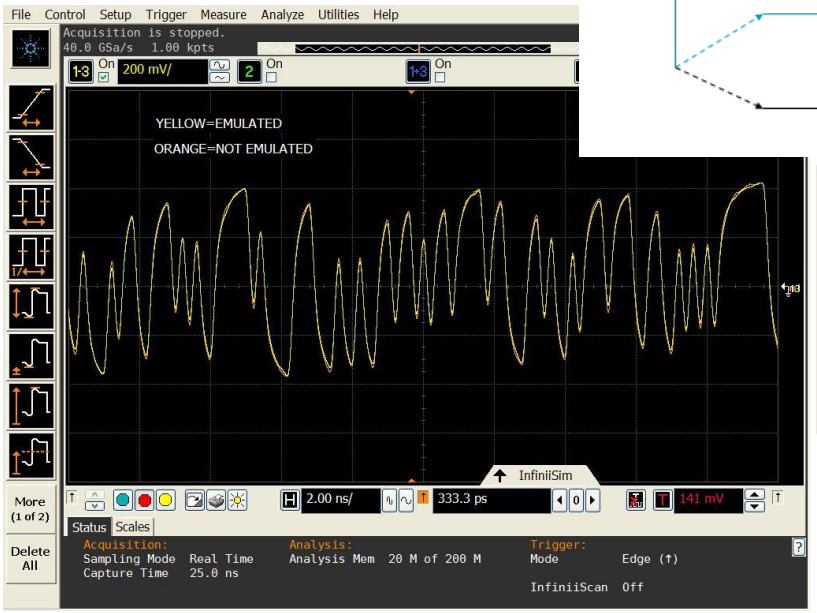
Agilent J-BERT
N4903B
5Gbps Output

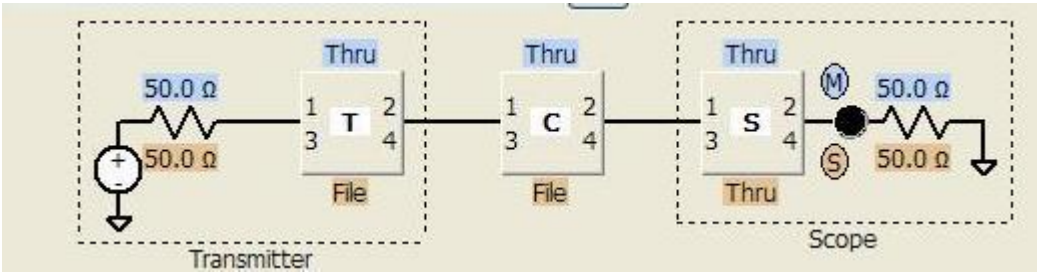
Compare!

Agilent T-Rex
DSA91304A

Compliance board and cable

S-para Emulation by Infiniisim

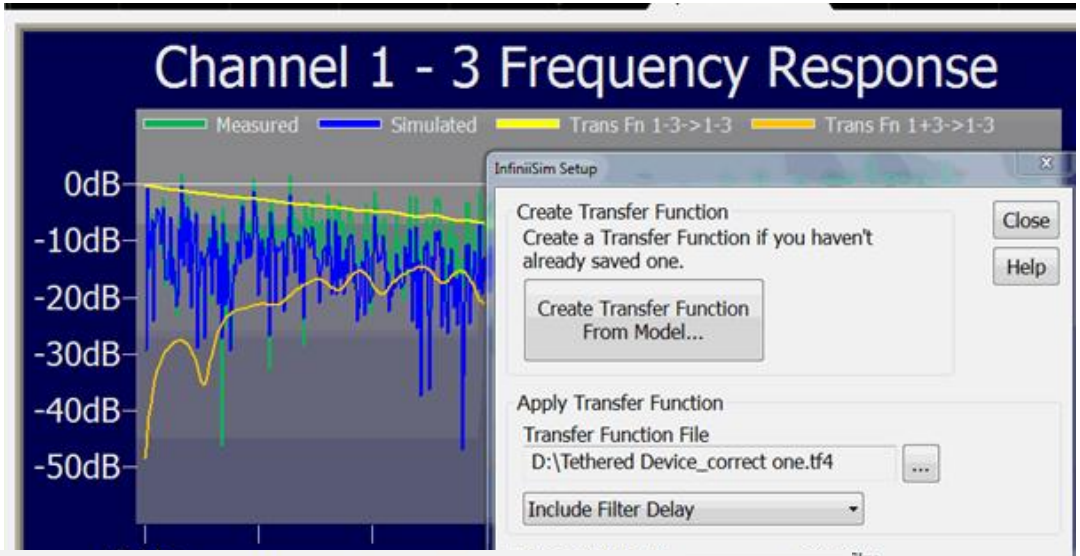


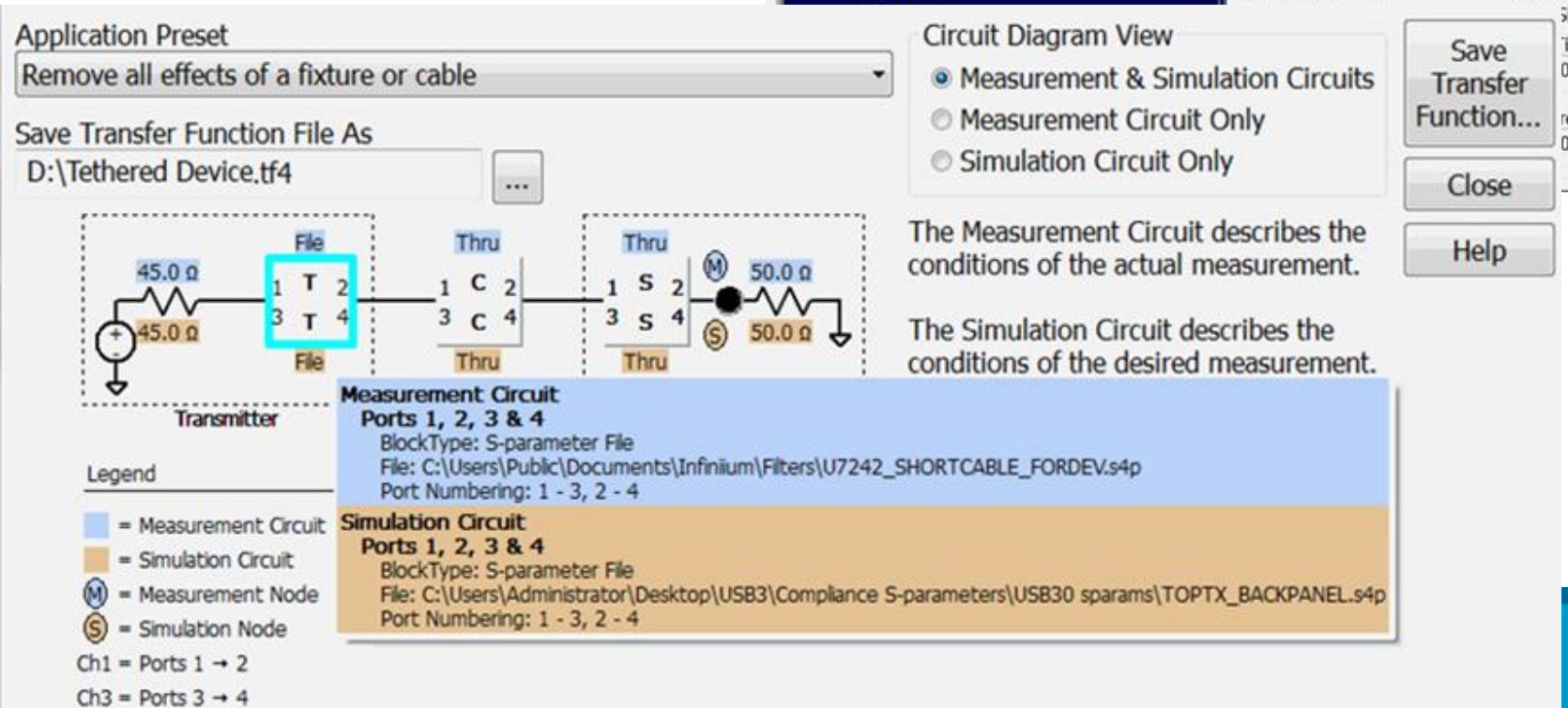


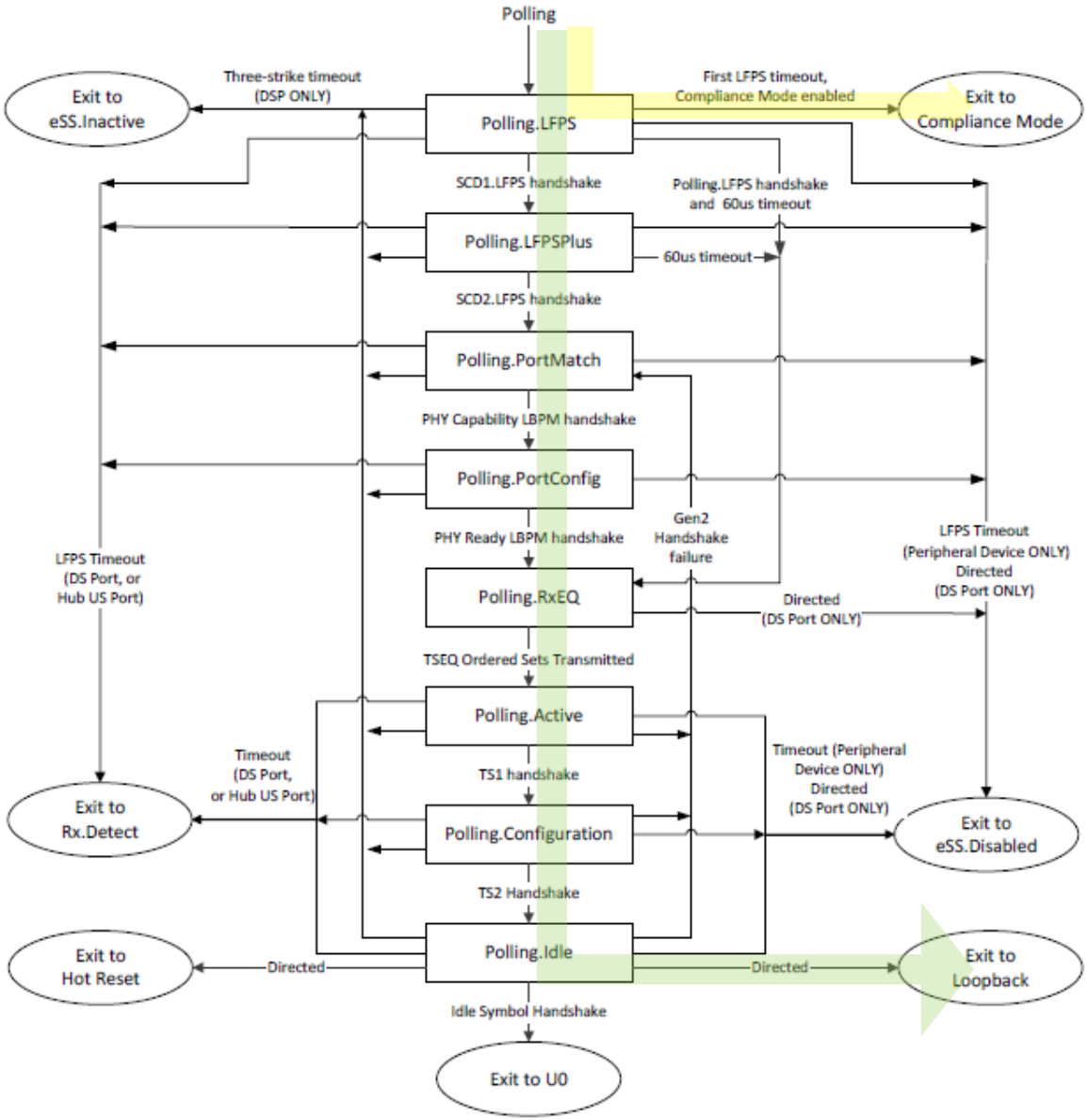
Validation with InfiniiSim of DSA91304A

InfiniiSim Creating Tethered Device Channel

- Import channel s-parameters
- Add channel loss – TopTX_Backpanel.s4p (simulate)
- Remove fixture loss – U7242_shortcable_forDev.s4p (measured)
- Result is Tethered TX response



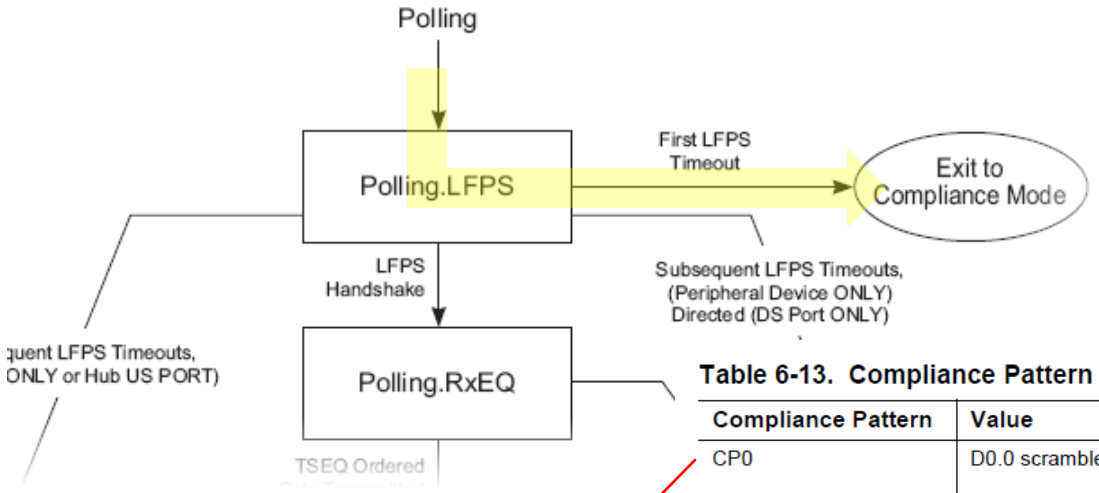




TX compliance modes

RX testing - loopback

TX Testing Requirements: Polling.LFPS to compliance mode



PING LFPS
Toggles CMM

CP0/9
Dj

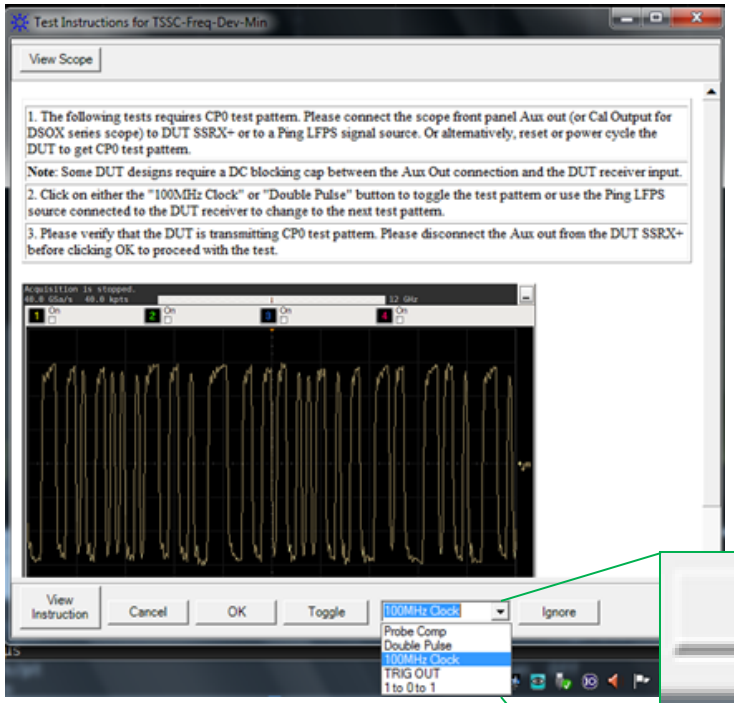
CP1/10
Rj

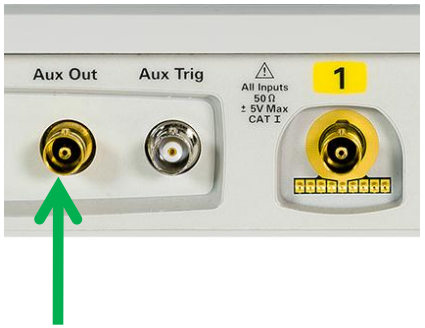
Table 6-13. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences.
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	With without de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP9		Pseudo-random data pattern (see section 6.4.4.1)
CP10	AAh	Nyquist pattern at 10Gb/s. This is not 128b132b encoded.
CP11	CCh	Nyquist/2 at 10Gb/s, This is not 128b132b encoded.
CP12	LFSR15	Uncoded LFSR15 for PHY level testing and fault isolation. This is not 128b132b encoded.

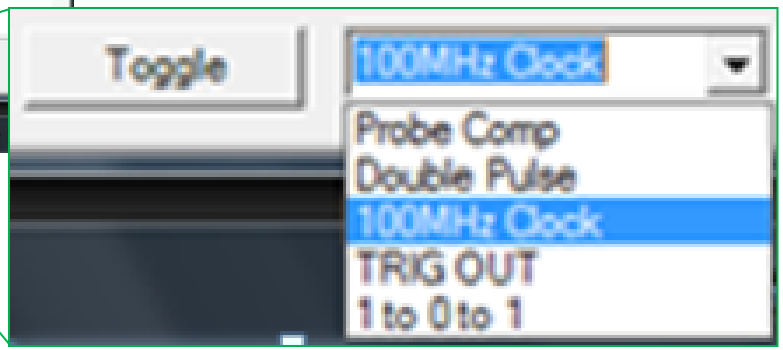
Note: Unless otherwise noted, scrambling is disabled for compliance patterns.

Toggling USB 3.0/3.1 TX test modes





- Connect Aux Out to DUT SSRX+ to toggle test modes
- For DSOX use Cal Out

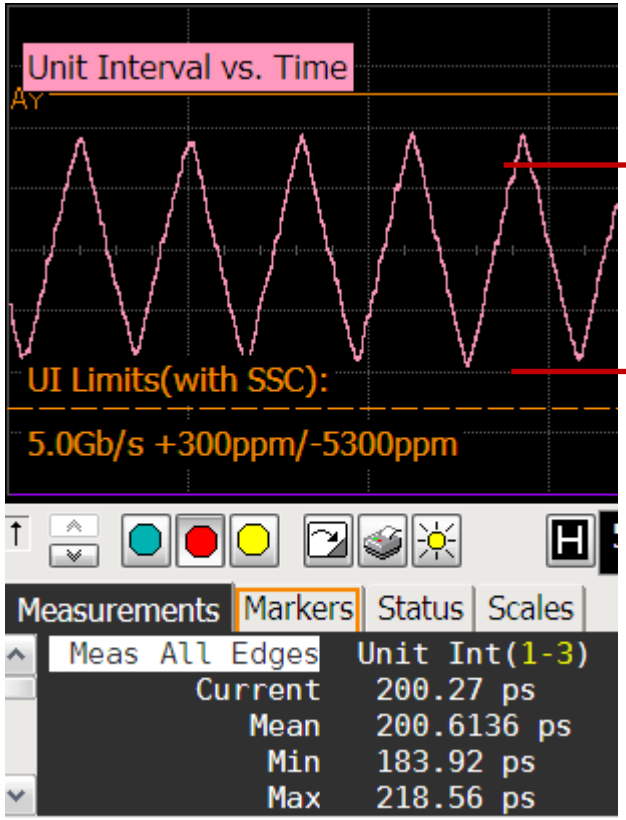


Additional methods to toggle TX test modes:

- Use differential output of N4903B JBERT
- 81134A PG
- Function Gen or AWG

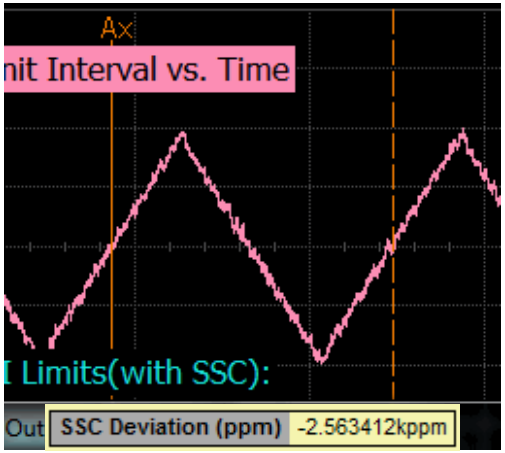
SSC will continue to be a challenge for USB 3.1

- Spread spectrum clocking is the intentional down-spreading of the transmitter's output data rate.



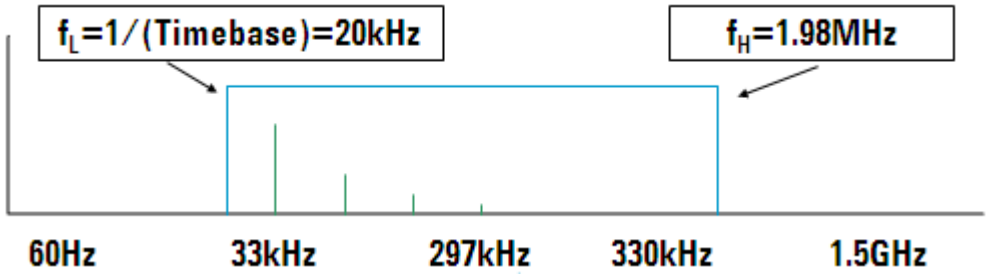
-3700ppm

-300ppm



ECN 15: Nom -2000ppm

We isolate the 30-33kHz SSC modulation frequency and its relevant harmonics



USB 3.0 Compliance Channels

Compliance Channels are used to test TX and RX for worst case channel conditions

Standard connector:

- Channel loss will dominate
- 11” PCB trace for device testing
- 5” PCB trace for host testing
- 3 meter USB 3.0 cable

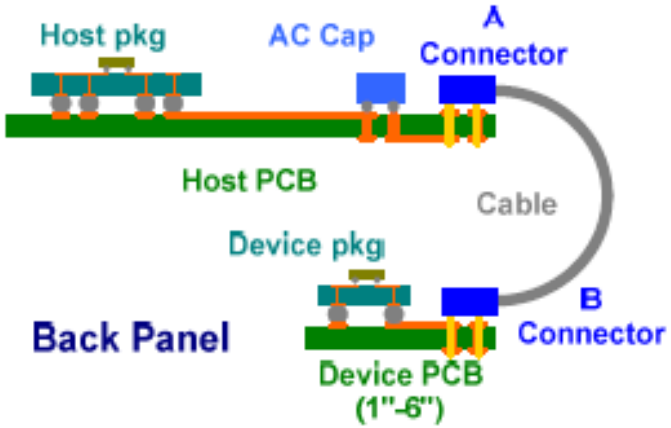
Micro connector:

- Channel loss will dominate
- 11” PCB trace for device testing
- 5” PCB trace for host testing
- 1 meter USB 3.0 cable

Tethered:

- Channel loss will dominate
- 11” PCB trace for device testing
- 5” PCB trace for host testing
- short USB 3.0 cable

Short Channel = no cable and shortest possible PCB traces

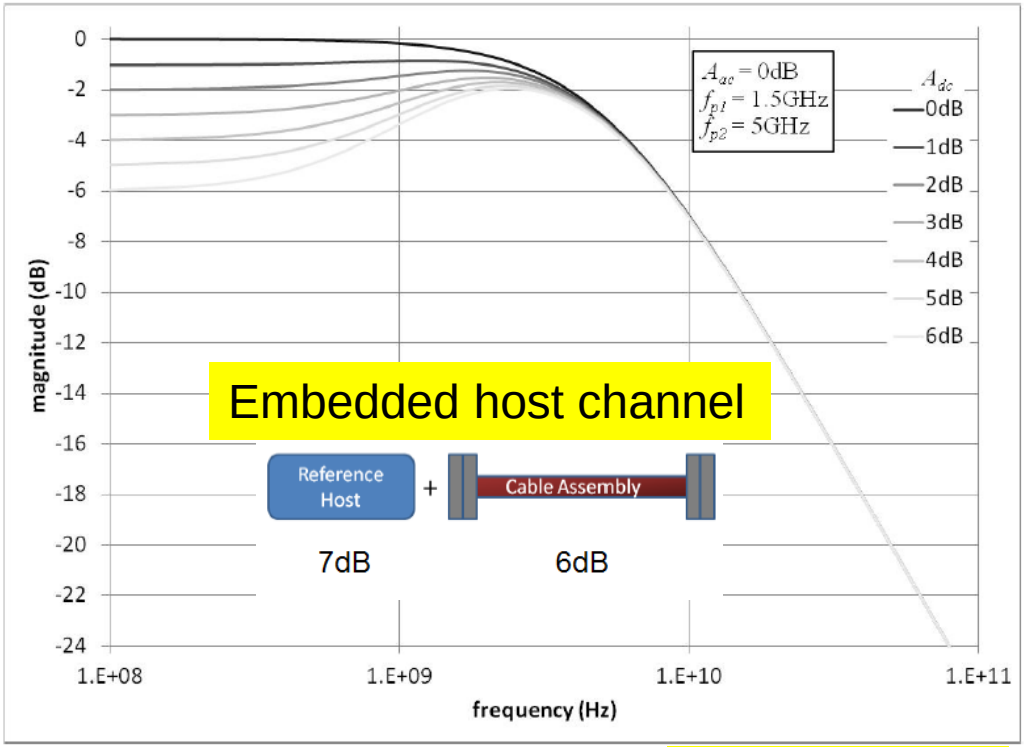


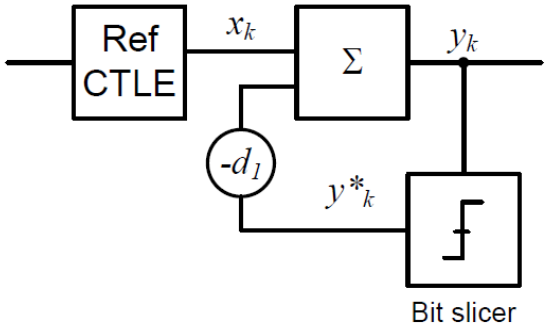
USB 3.1 Compliance Channels

- Die to die target is 20dB @ 5Ghz
- Host/dev exceeding 7dB may need repeater

7dB 6dB 7dB

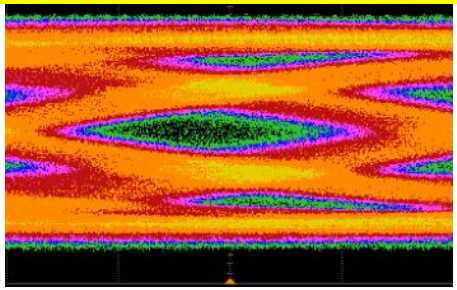
USB 3.1 Reference Equalizer



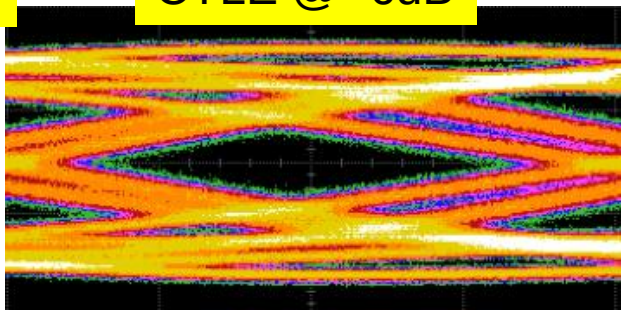


Ref CTLE + 1 tap DFE

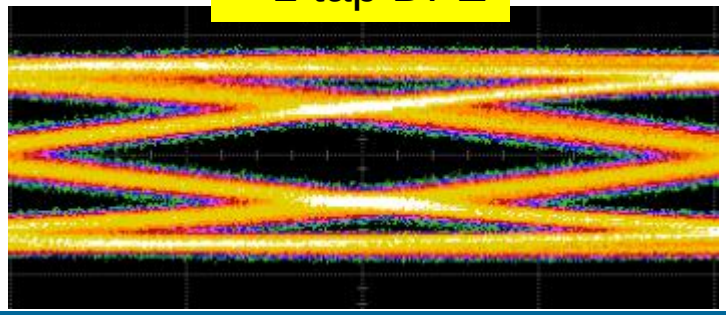
Eye at end of Channel



CTLE @ -6dB



+ 1 tap DFE



USB 3.1 10G Channel Budgets

- Full channel budget of 20 dB at 5Ghz
- Symmetric loss for host and device
- TX EQ settings informative only
  - Passing the limits at end of channel will dictate TX settings
  - For short channels settings similar to USB 3.0 5G likely
  - Lossy channels near max specified likely to need pre/post cursor
- Repeaters will be more common for longer channels

Receiver Testing Topics

- Low Frequency Periodic Signaling (LFPS)
- Loopback
- Jitter Tolerance
- J-BERT SSC setup
- N5990A Test Automation SW

LFPS – SCD1 & SCD2 – tRepeat Modulation

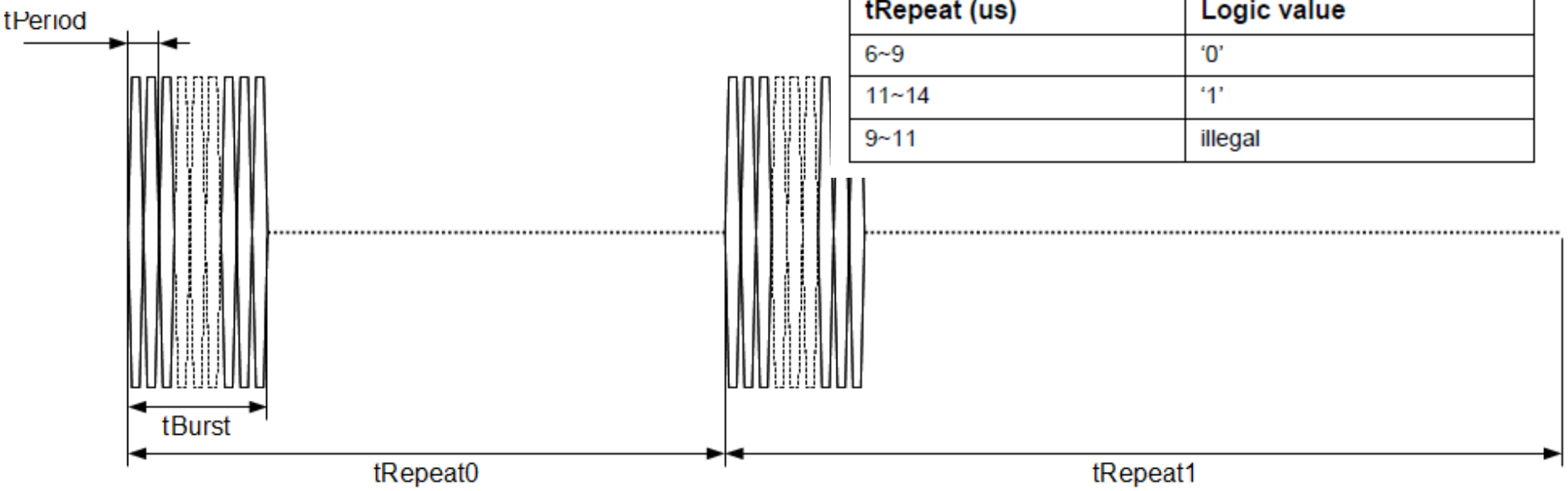
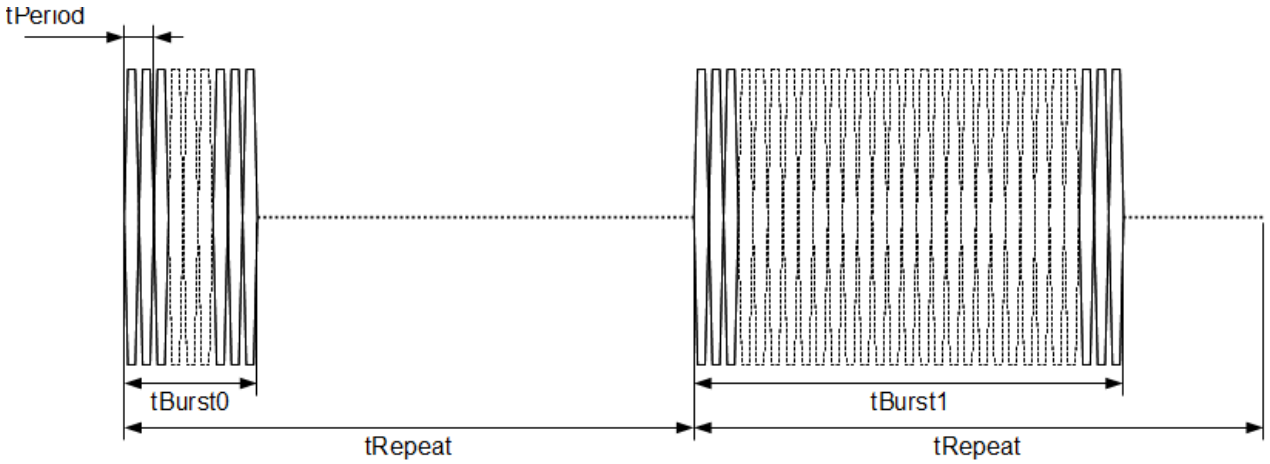


Table 6-31. Binary Representation of Polling.LFPS

tRepeat (us)	Logic value
6~9	'0'
11~14	'1'
9~11	illegal

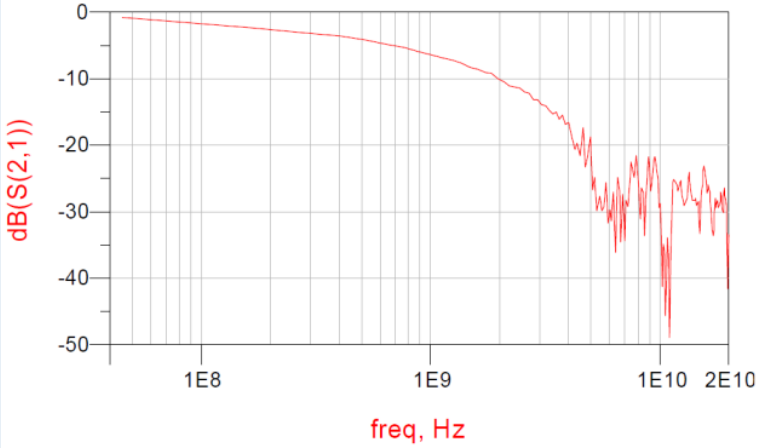
- tRepeat is modulated to express 0 (short) and 1 (long)
- SCD1.LFPS (4'b0100), and SCD2.LFPS (4'b1101)
- SuperSpeed+ identity check

LFPS Based PWM Signaling (LBPM) Encoding

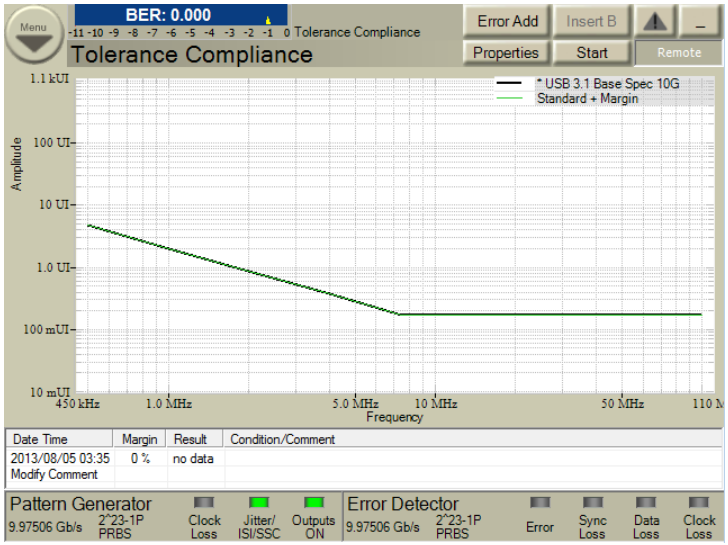


- Rate (speed and lane) announcement and negotiation
- Repeater declaration
- Power state transition in repeater
- Can be expanded to:
  - VBus control on/off, overcurrent sensing
  - Power delivery
  - Vendor specific operation

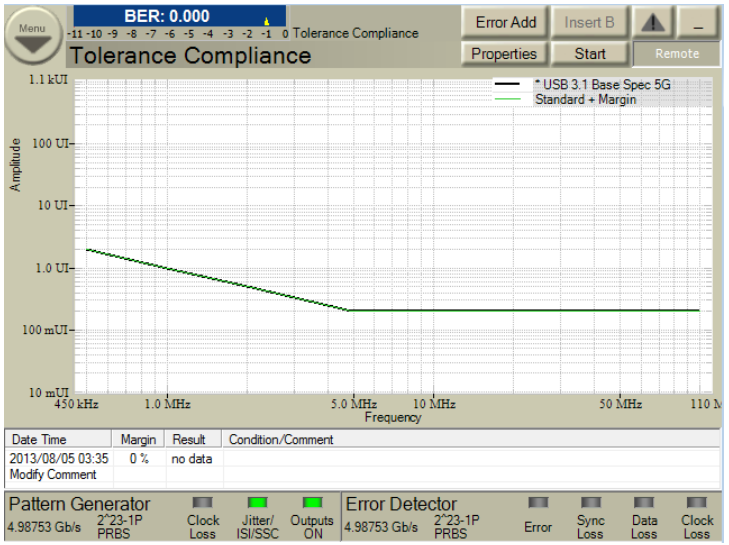
Jitter Tolerance – Stress Components – Base Spec

	Gen1 5G	Gen2 10G
TJ after RX EQ	450mUI	394mUI
RJ_{rms} / $RJ_{pp\ ber=1E-12}$	12.1mUI / 177.9mUI	13.08mUI / 192.3mUI
$SJ_{out\ of\ CDR\ tracking\ range}$	200mUI	170mUI
Channel	channel -20.6dB @ 5GHz ➔ J20 24” trace is very close 	

Jitter Tolerance Settings – Base Spec

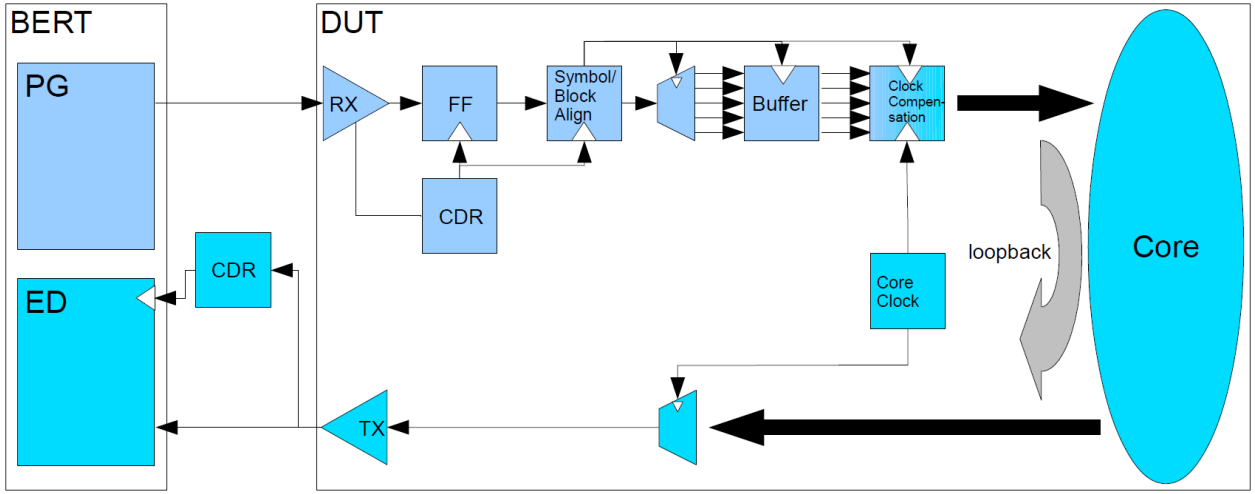


- Center Data Rate with SSC: 9.975Gb/s
- SSC: Center Spread 33kHz with 0.25%
- Voltage Swing @ TP1: 800mV
- Pre-shoot @ TP1: 2.7dB
- De-Emphasis @TP1: -3.3dB
- RJ: 1.308ps RMS
- channel -20.6dB @ 5GHz ➔ J20 24” trace is very close



- Center Data Rate with SSC: 4.9875Gb/s
- SSC: Center Spread 33kHz with 0.25%
- Voltage Swing @ TP1: 750mV
- De-Emphasis @TP1: -3.0dB
- RJ: 2.42ps RMS
- channel -20.6dB @ 5GHz ➔ J20 24” trace is very close

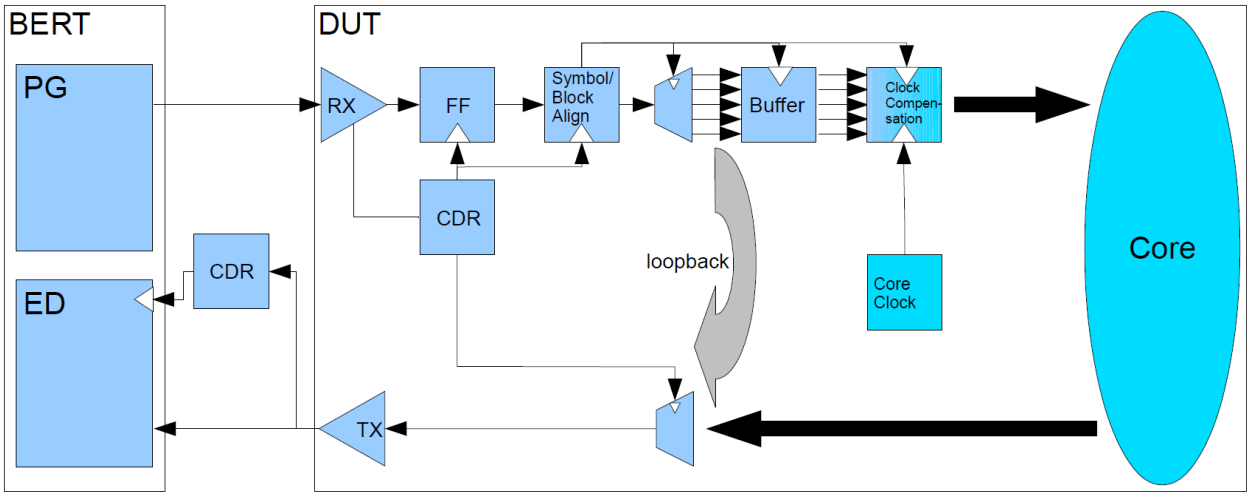
Loopback – Filter SKPOS



- Modification is within SKPOS only

➔ BERT ED needs to filter SKPOS on expected as well as received pattern and compare remaining bits

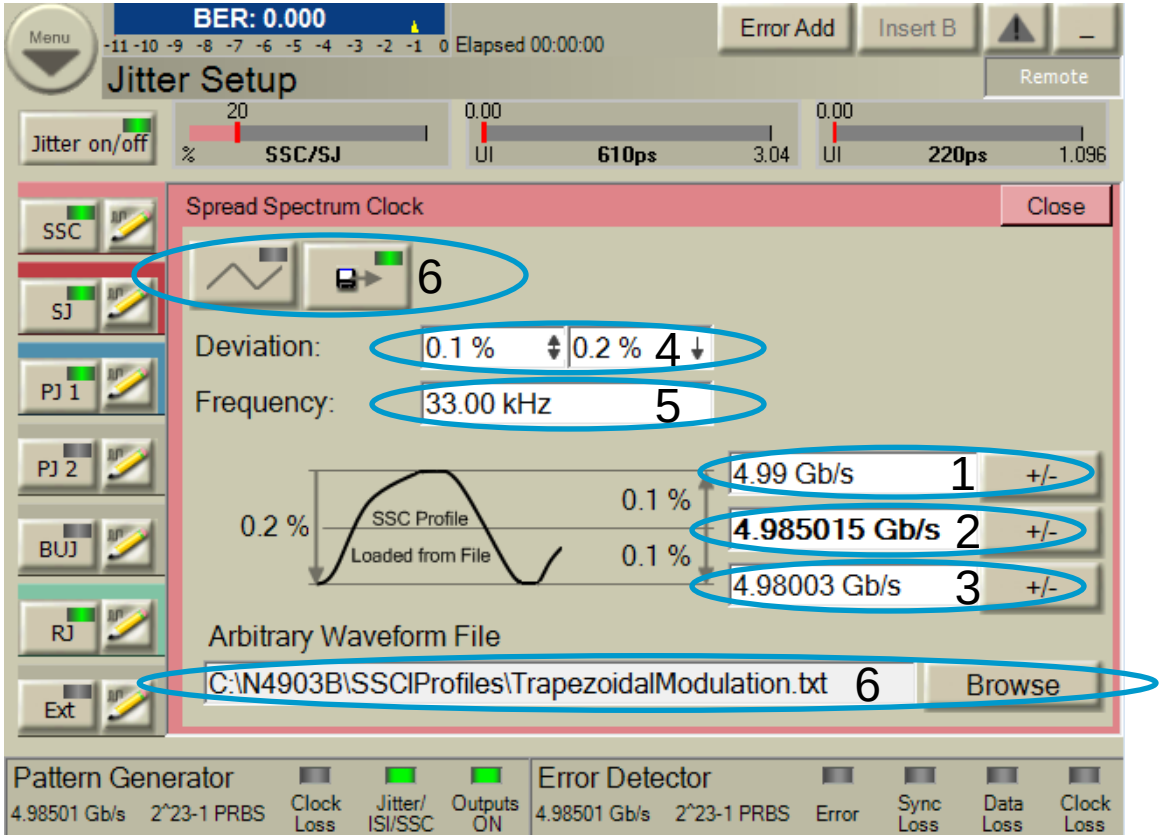
Loopback – Analog Loopback



Early PHY only testing available by using analog loopback

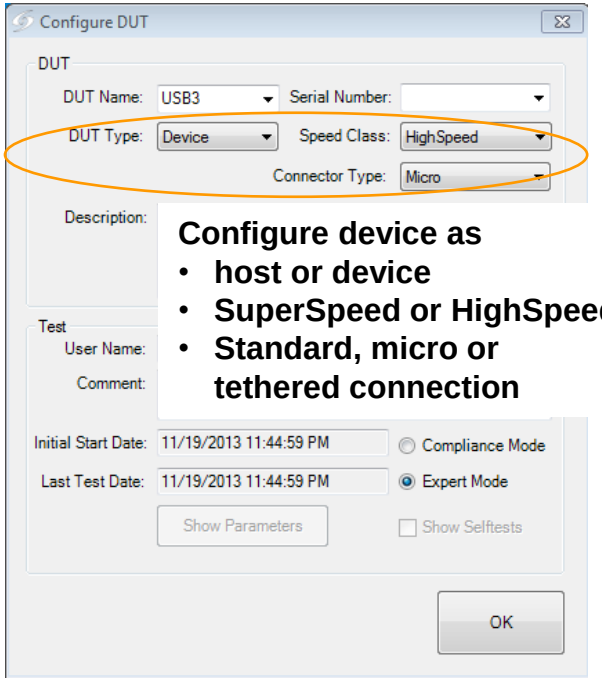
- ➔ analog loopback bypasses the clock compensation and both the DUT RX as well as the DUT TX run in the BERT's clock domain
- ➔ The DUT does not modify the pattern and normal BER comparison can be used
- ➔ BUT since the DUT uses the clock recovered by the RX to clock the TX jitter is transferred back to the BERT ED. Choose BERT ED clocking with respect to DUT jitter transfer characteristics

J-BERT SSC Setup and Capabilities

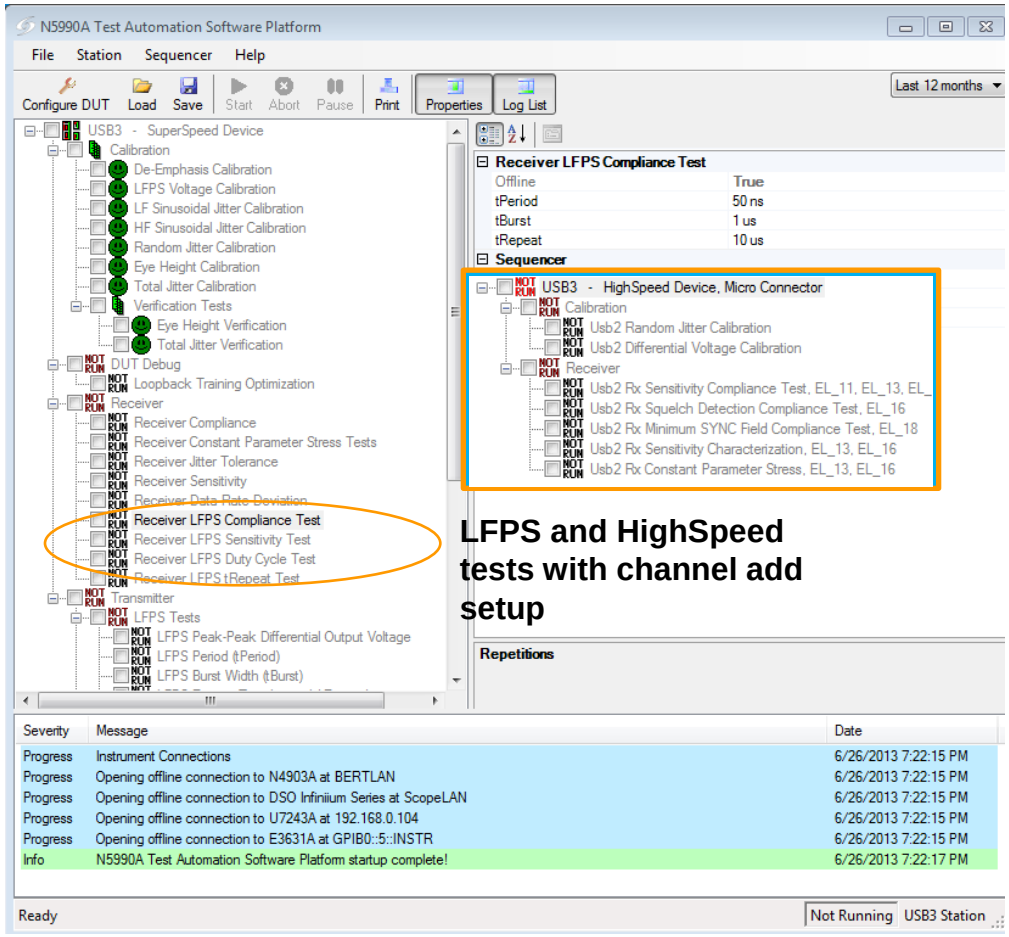


1. Upper data rate
2. Center data rate
3. Lower data rate
4. Deviation
5. Modulation Frequency
6. Arbitrary modulation profiles or standard triangular. Arbitrary profiles can be used to for Lexmark or Hershey Kiss profiles or to use profiles captured from a real DUT using a real time scope

N5990A USB 3.0 Test Automation SW



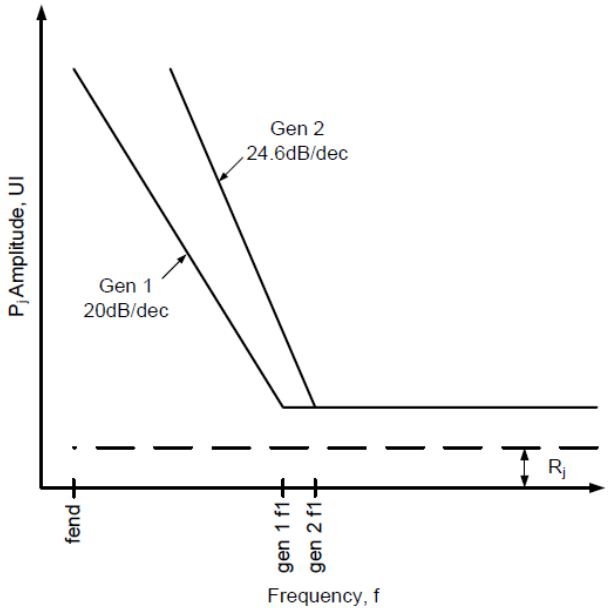
Configure device as
- **host or device**
- **SuperSpeed or HighSpeed**
- **Standard, micro or tethered connection**



LFPS and HighSpeed tests with channel add setup

SuperSpeed Receiver Tests
Rx Compliance and Jitter Tolerance Testing

- Automated instrument control for:
  - Setup calibration
  - Compliance test
  - Characterization test
  - Support for debugging
- Operator guidance
- Sophisticated test reports
- Controls J-BERT, Oscilloscope.
- Supports full product characterization including transmitter measurements



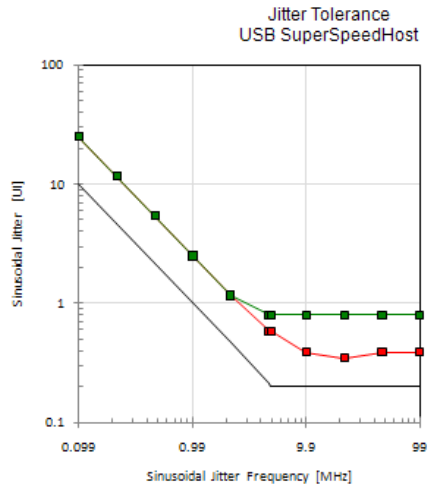
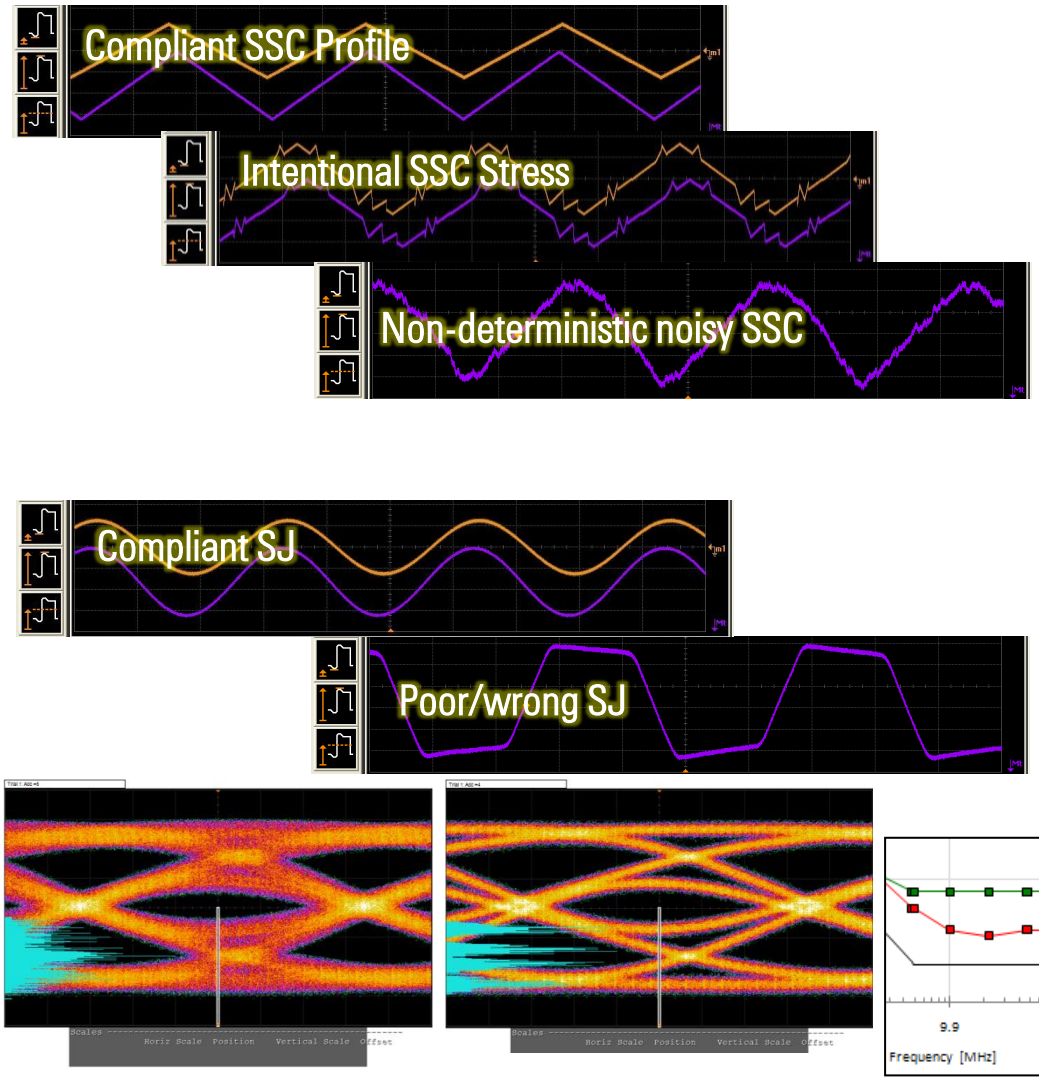


Figure 6-28. Jitter Tolerance Curve

Result	SJ Frequency [MHz]	Failed Jitter [UI]	Passed Jitter [UI]	Min Spec [UI]	Symbol Errors
pass	0.500		2.00	2.000	0
pass	1.000		1.00	1.000	0
pass	2.000		0.50	0.500	0
pass	4.900		0.20	0.200	0
pass	10.000		0.20	0.200	0
pass	20.000		0.20	0.200	0
pass	33.000		0.20	0.200	0
pass	50.000		0.20	0.200	0

Biggest Challenges for USB 3.1 Physical Layer Testing

- Transmitter SSC quality
  - SSC ECNs
  - Interference issues
- Loopback issues
  - Dut needs custom sequence
  - DUT drops out easily
- Calibration issues
  - Inconsistent
  - Poor Sj/Rj mod
  - Automation of Cal
- RX and TX Equalizer Tuning
- Jitter tolerance failures

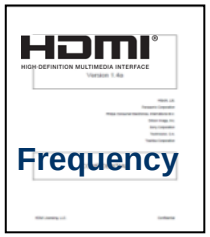


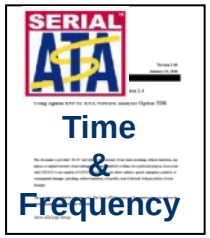
ENA Option TDR Compliance Test Solution

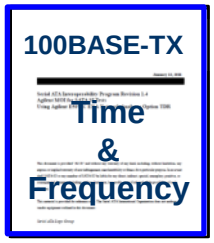
Certified Method of Implementation (MOI)

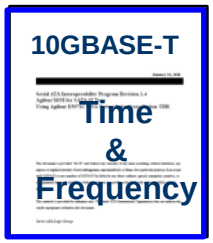
Compliance test solutions (i.e. certified MOIs) for ENA Option TDR are available at **www.agilent.com/find/ena-tdr_compliance**

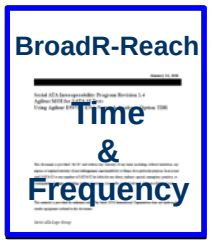
Cable / Connector











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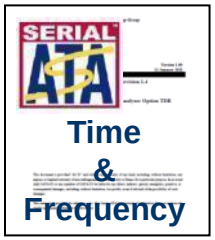
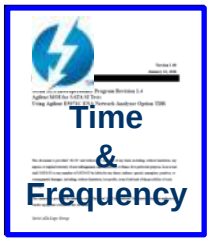
Transmitter/Receiver (Hot TDR)





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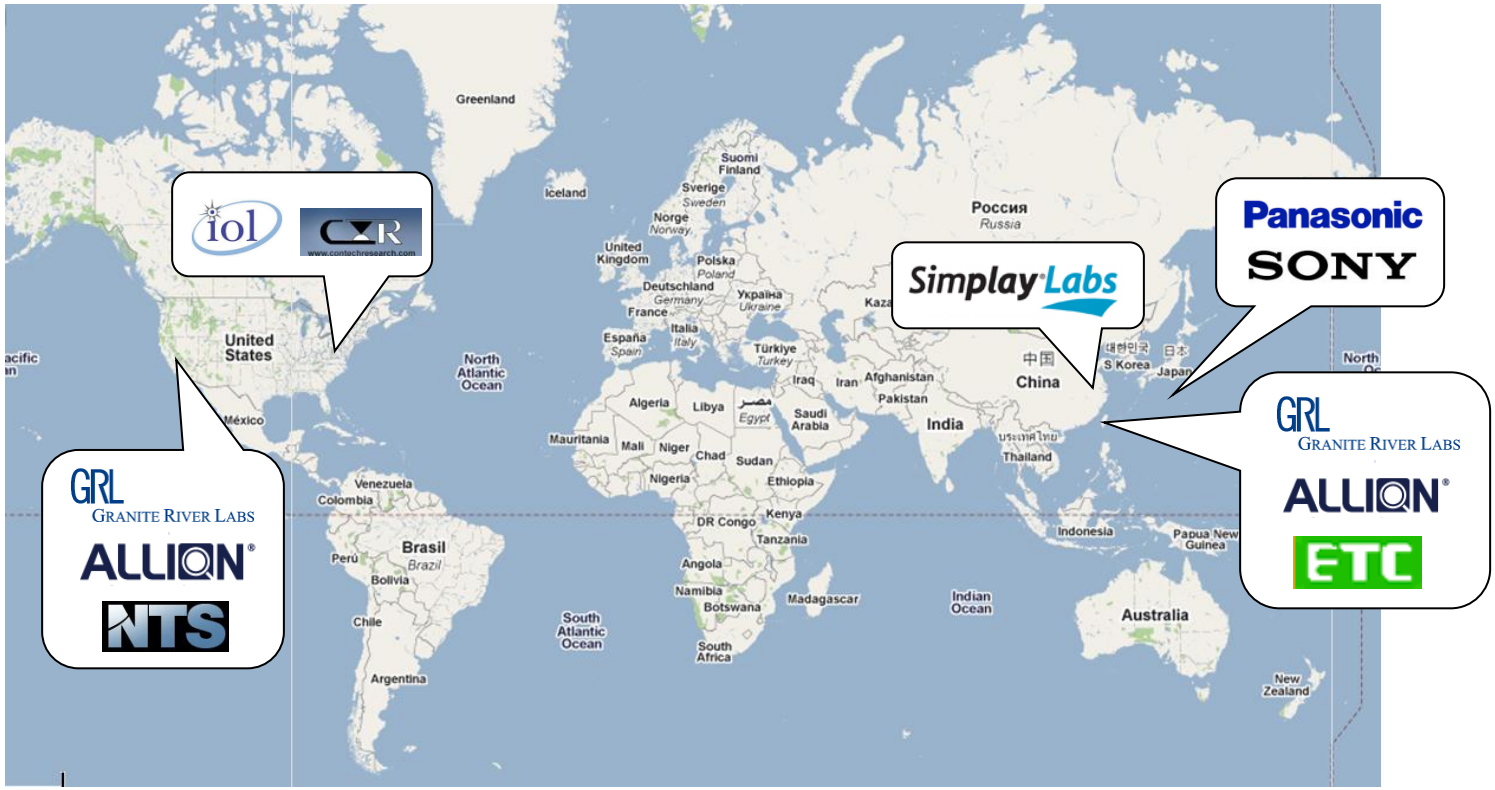
ENA Option TDR Compliance Test Solution

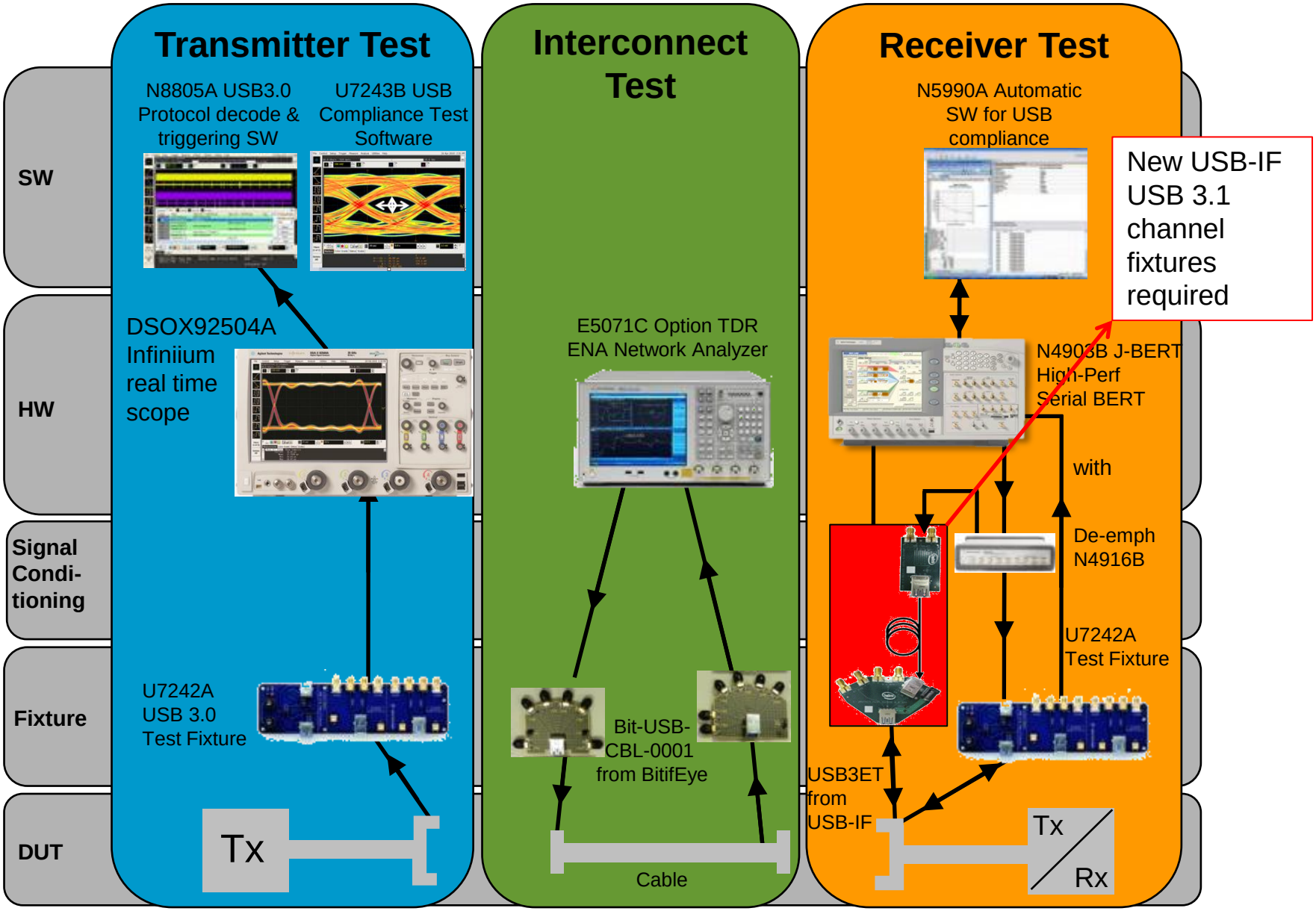
Certified Test Centers using ENA Option TDR

Test Centers Support ENA Option TDR

ENA Option TDR is used world wide by certified test centers of USB, HDMI, DisplayPort, MHL, Thunderbolt and SATA.



USB 3.1 – Total Solution



Summary

- USB-IF compliance tests and requirements have changed over time. Be sure to check for updates and ECNs at http://www.usb.org/developers/docs/
- USB 3.0 and 3.1 Receiver testing will continue to be the most challenging part of PHY layer testing
- Agilent USB solutions adopted by test labs world wide
  - Confidence in our solution comes from our leadership and participation in standards bodies as well as our deep technical expertise
- 10G SuperSpeed USB 3.1 will bring exciting new performance capabilities to product developers next year and beyond

Agilent has the tools and expertise to help you conquer USB 3.1 Physical Layer Test Challenges

Additional Links and References

Agilent Oscilloscope information (TX testing solutions)

www.agilent.com/find/scopes

Agilent Oscilloscope application software

http://www.home.agilent.com/agilent/product.jspx?nid=-35491.0.00&cc=US&lc=eng

Agilent N4903B Jbert (Rx testing solutions)

www.agilent.com/find/JBERT

Agilent N8900A InfiniiView Oscilloscope Analysis Software

www.agilent.com/find/InfiniiView

Agilent N2809A PrecisionProbe oscilloscope probing software

www.agilent.com/find/precisionprobe