



HDMI®

HIGH-DEFINITION MULTIMEDIA INTERFACE



Contents

-Introduction of HDMI

- What is HDMI?
- TMDS

-HDMI 1.4 Test

- Source Test
- Sink Test
- Cable Test

-HDMI 1.4 Source Test

-HDMI 2.0

-HDMI 2.0 Test

- Source Test
- Sink Test

HDMI

De facto digital interface standard

- HDMI, which stands for High-Definition Multimedia Interface, is the de facto digital interface standard for connecting HD consumer electronics components.
- HDMI enables consumer electronics and PC manufacturers to bring to market innovative and feature-rich products that enhance the quality of a consumer's high-definition experience.



Why HDMI?



BEFORE

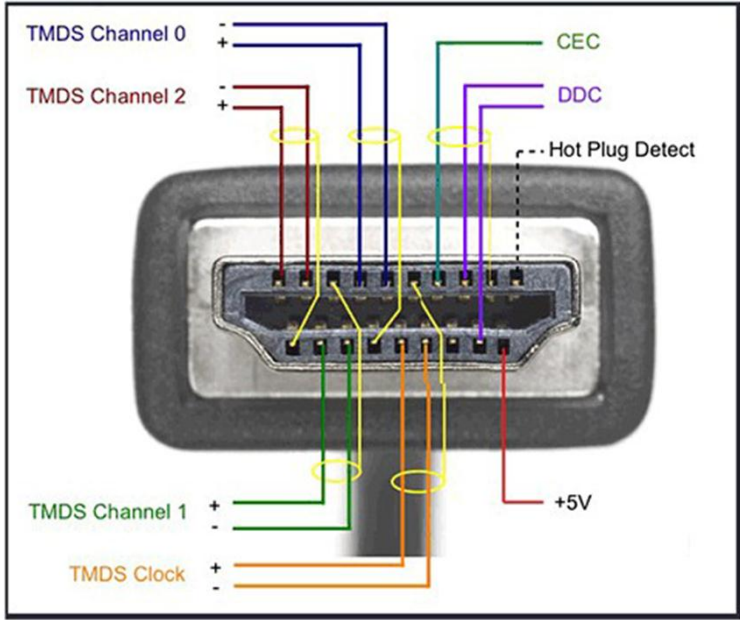
DVD Player, Set-top box, & AV Receiver



AFTER

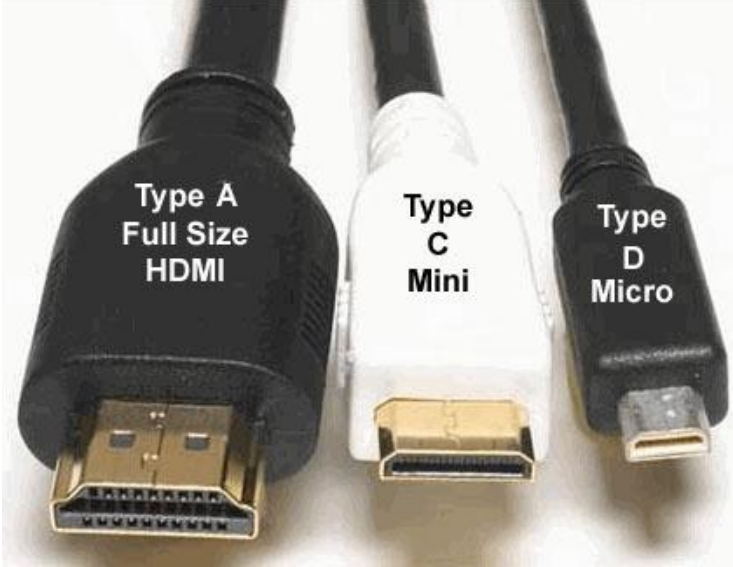
Equivalent functions
Higher performance

Plug Technologies

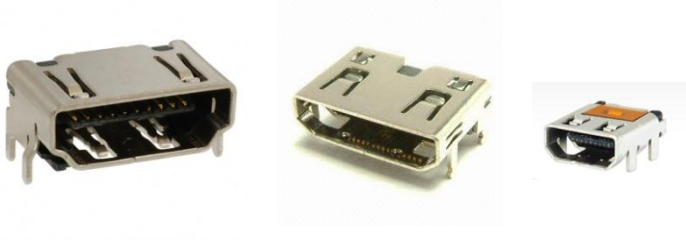


19-pin plug supports:

- 3 TMD channels
- Clock
- DDC channel
- CEC channel
- +5V power
- Hot plug detect



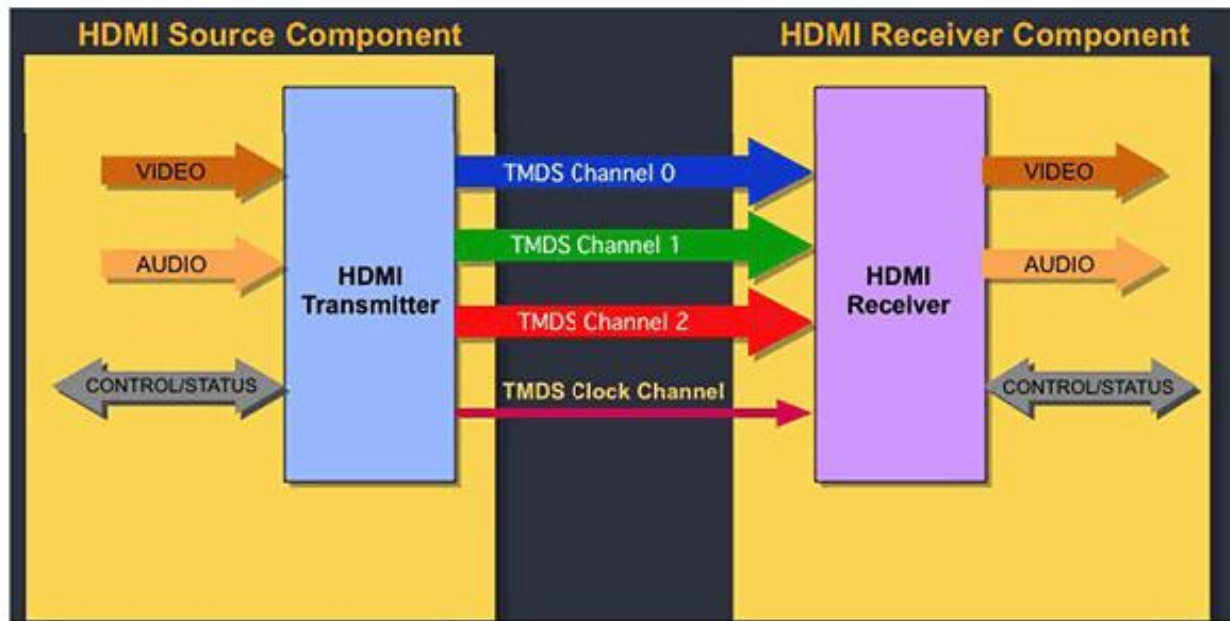
Plug



Receptacle

Video/Audio

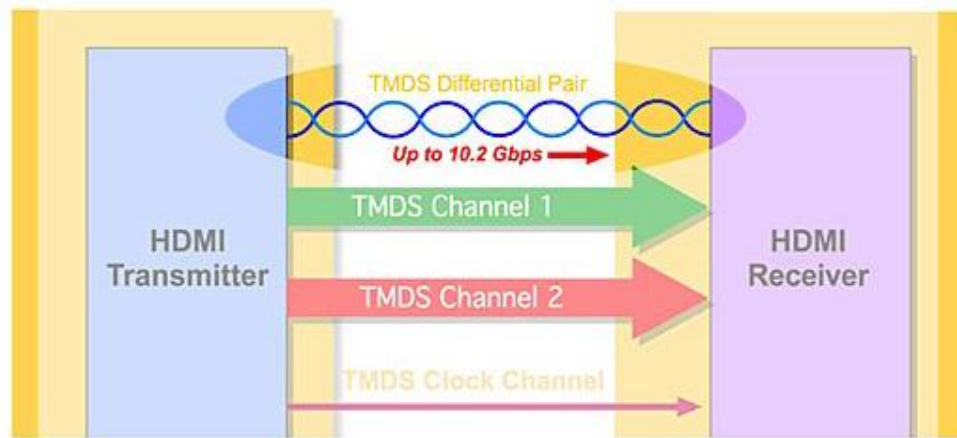
- Three High speed video/audio data channels
 - Data rates up to 10.2Gbps
 - Carries from 24 to 48-bit RGB/YCbCr video components
 - Digital audio and control data
- Clock channel – data recovery reference for receiver



Channel Signaling

■ TMDS

- Transition Minimized Differential Signaling
- Differential low-voltage signaling technology capable of supporting up to 10.2 Gbps total bandwidth

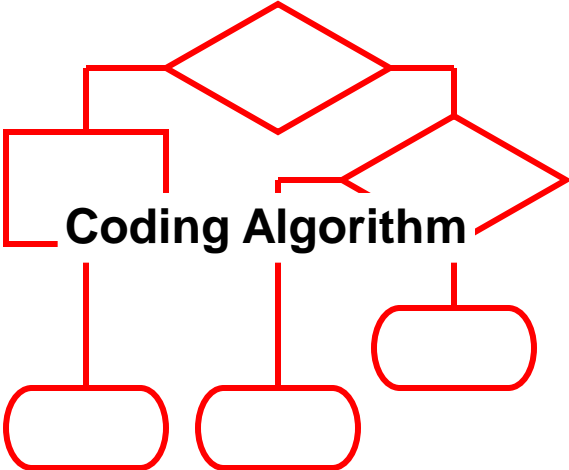


HDMI Physical layer

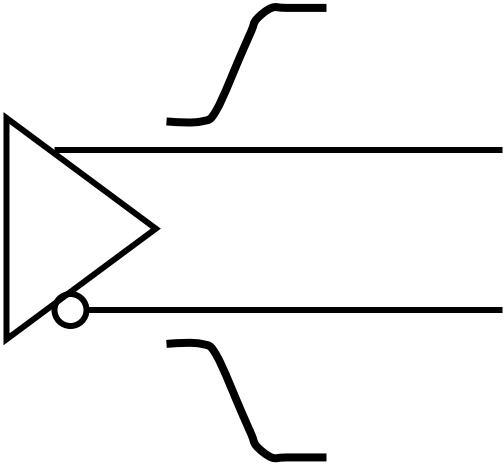
T.M.D.S.

(Transition Minimized Differential Signaling)

Minimized changing
between 0 and 1



Differential
Signal

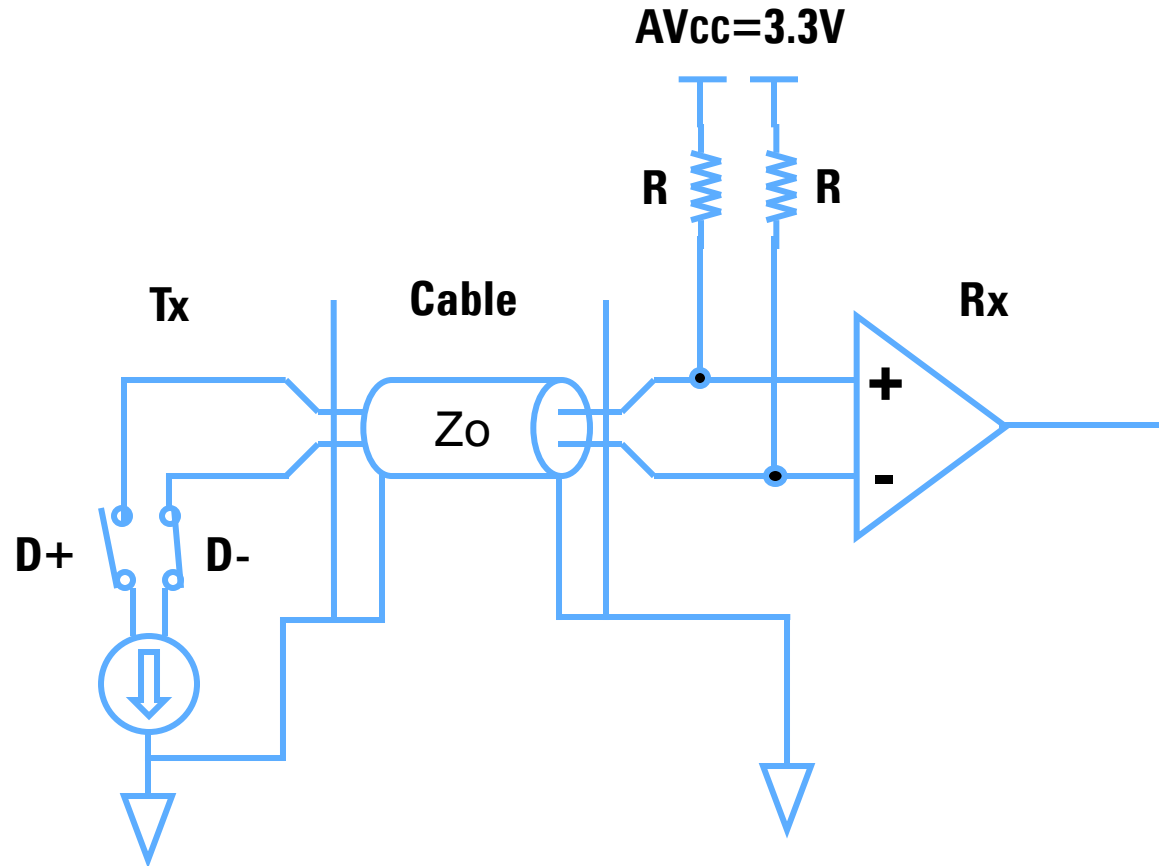


TMDS

Open drain
Current Drive

Differential 100
ohm Transfer
channel

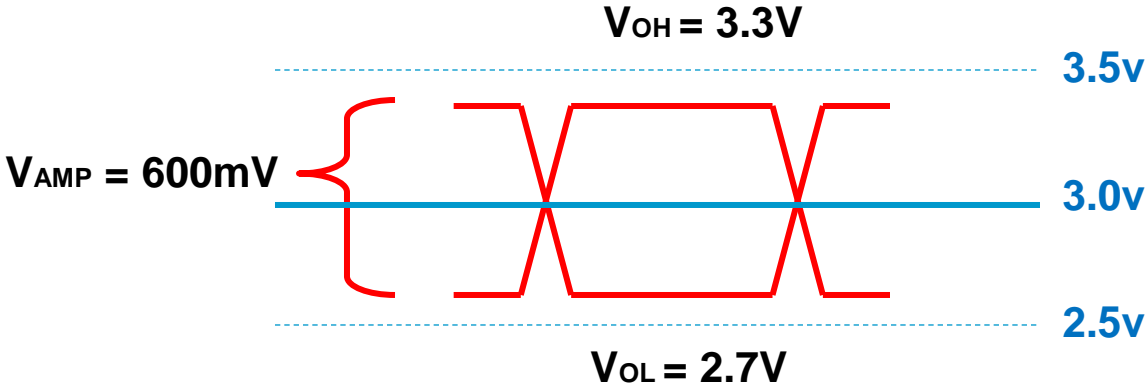
Center tap R
= 50Ω
Terminal voltage
: 3.3V



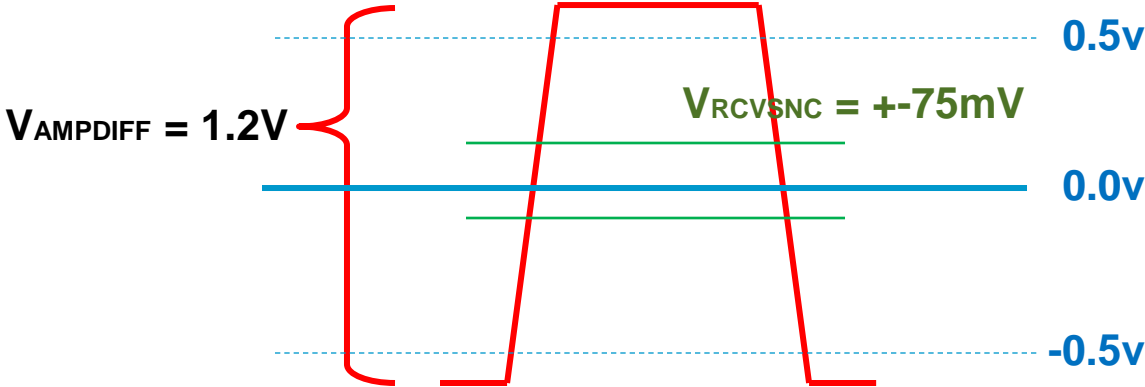
T.M.D.S. Link → 3.3V offset Termination, 3.4Gbps $T_r(20-80) = 75ps$

Signal Characteristic

Single ended



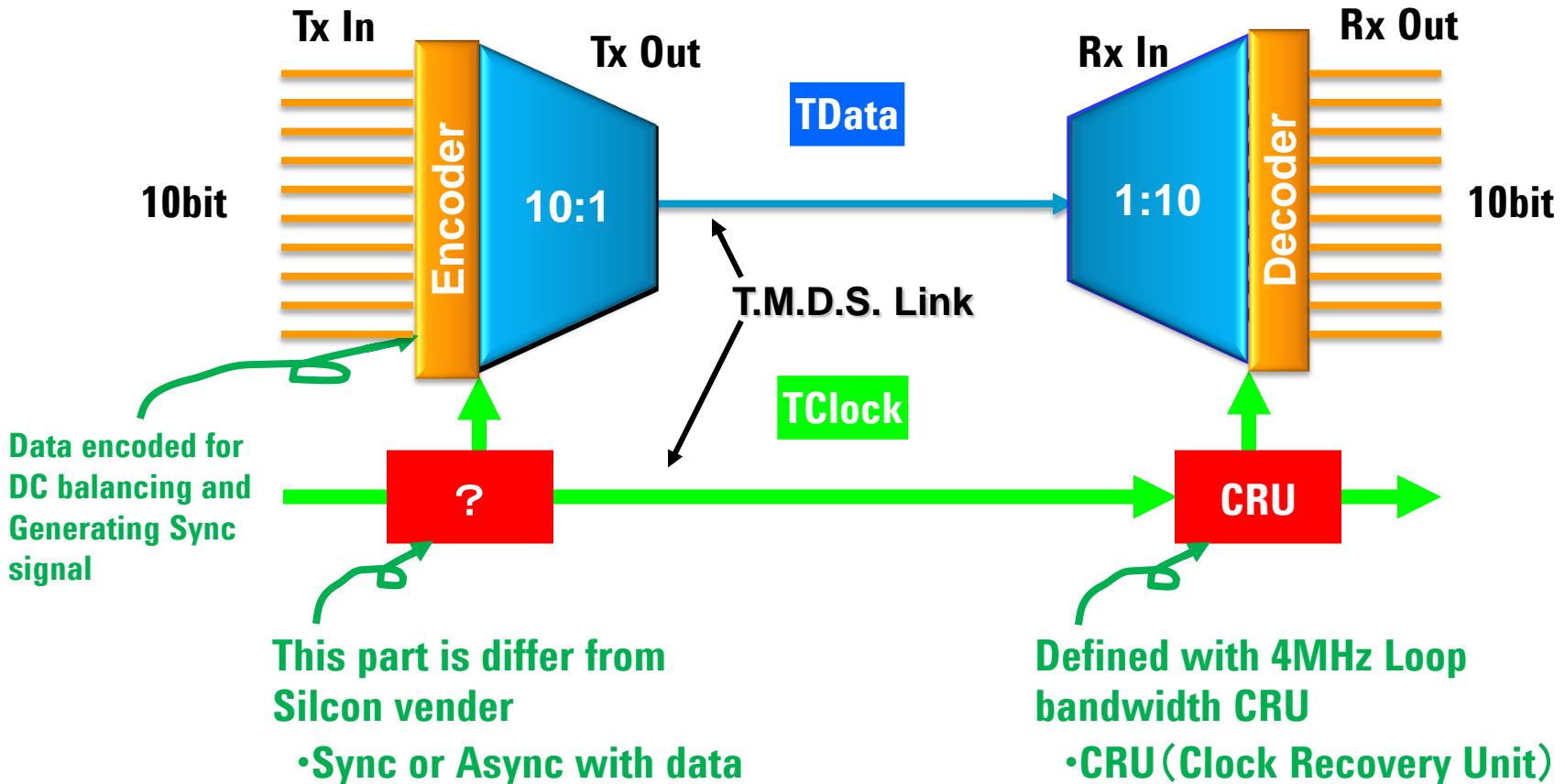
Differential



Signal Characteristic(cont')

- Data Rate : 250 Mbps to 3.4 Gbps
- Pixel Clock Frequency : 25 MHz to 340 MHz
- Rise/Fall Time : < 75 ps (RT/FT=20% to 80%)
- Vswing : 800mV to 1.2V
- T_{bit} : 294 ps to 4 ns
- V_{low} (single ended) : $AV_{\text{cc}}-600\text{mV} \leq V_{\text{low}} \leq AV_{\text{cc}}-400\text{mV}$
- V_{high} (single ended) : $AV_{\text{cc}} \pm 10\text{mV}$

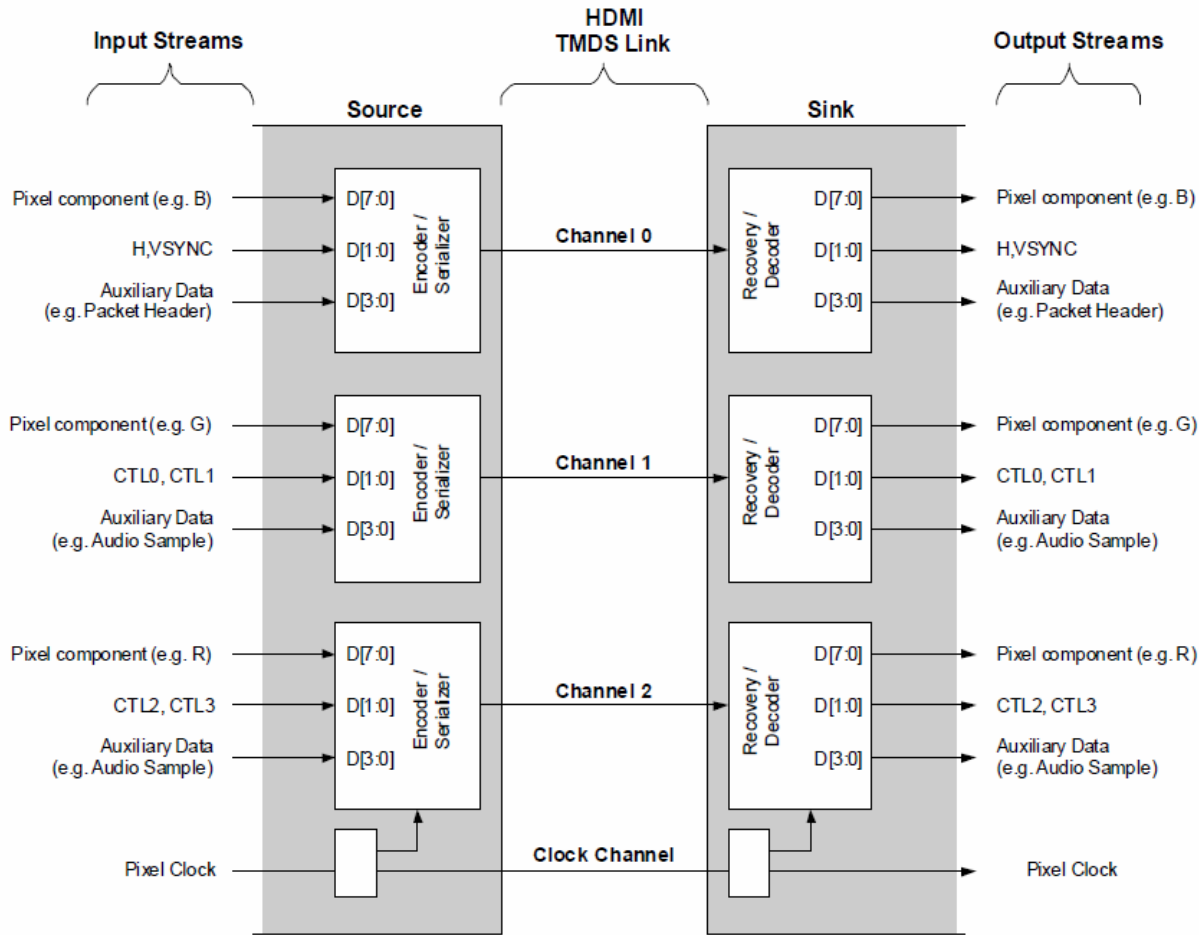
SerDes Structure – TMD5 Link



Depend on each of Tx/Rx , allowed Jitter is differ

So, Interoperability test are need between other benders

HDMI Encoder/Decoder overview

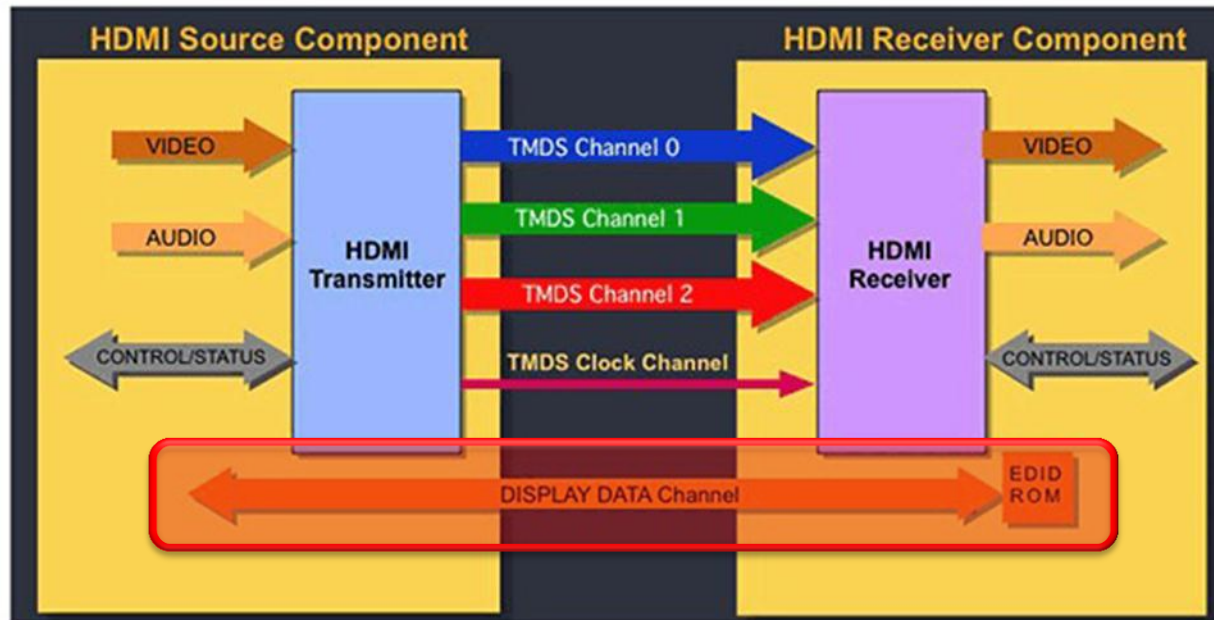


In case of 1080p , sending more than 30channels with 148.5MHz clock sync hronization

Parallel part also be High speed and Multi channels

Display Data Channel (DDC)

- Transfer display data using VESA Standard
- EDID – Extended Display Identification Data



EDID (Extended Display Identification Data)

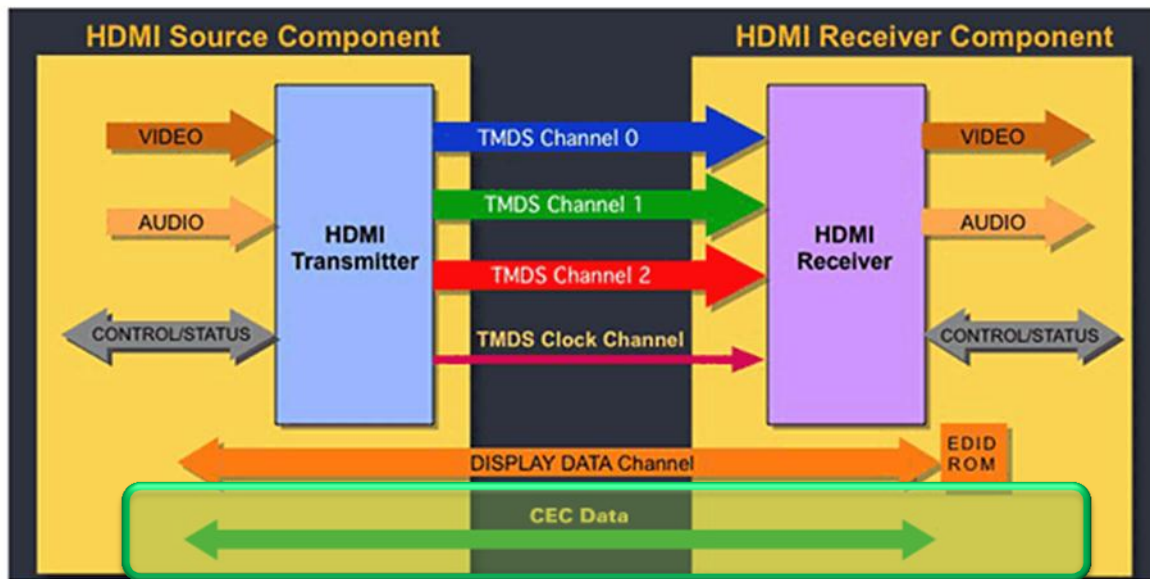
Monitor Name	EPI EnVision EN-775e
Monitor ID	EPID775
Model	EN-775e
Manufacture Date Week	26 / 2002
Serial Number	1226764172
Max. Visible Display Size	32 cm x 24 cm (15.7")
Picture Aspect Ratio	4:3
Horizontal Frequency	30 - 72 kHz
Vertical Frequency	50 - 160 Hz
Maximum Resolution	1280 x 1024
Gamma	2.20
DPMS Mode Support	Active-Off
Supported Video Modes:	
640 x 480	140 Hz
800 x 600	110 Hz
1024 x 768	85 Hz
1152 x 864	75 Hz
1280 x 1024	65 Hz
Monitor Manufacturer:	Envision, Inc.

**Sample EDID information
Sent from display**

CEC (Consumer Electronic Control)

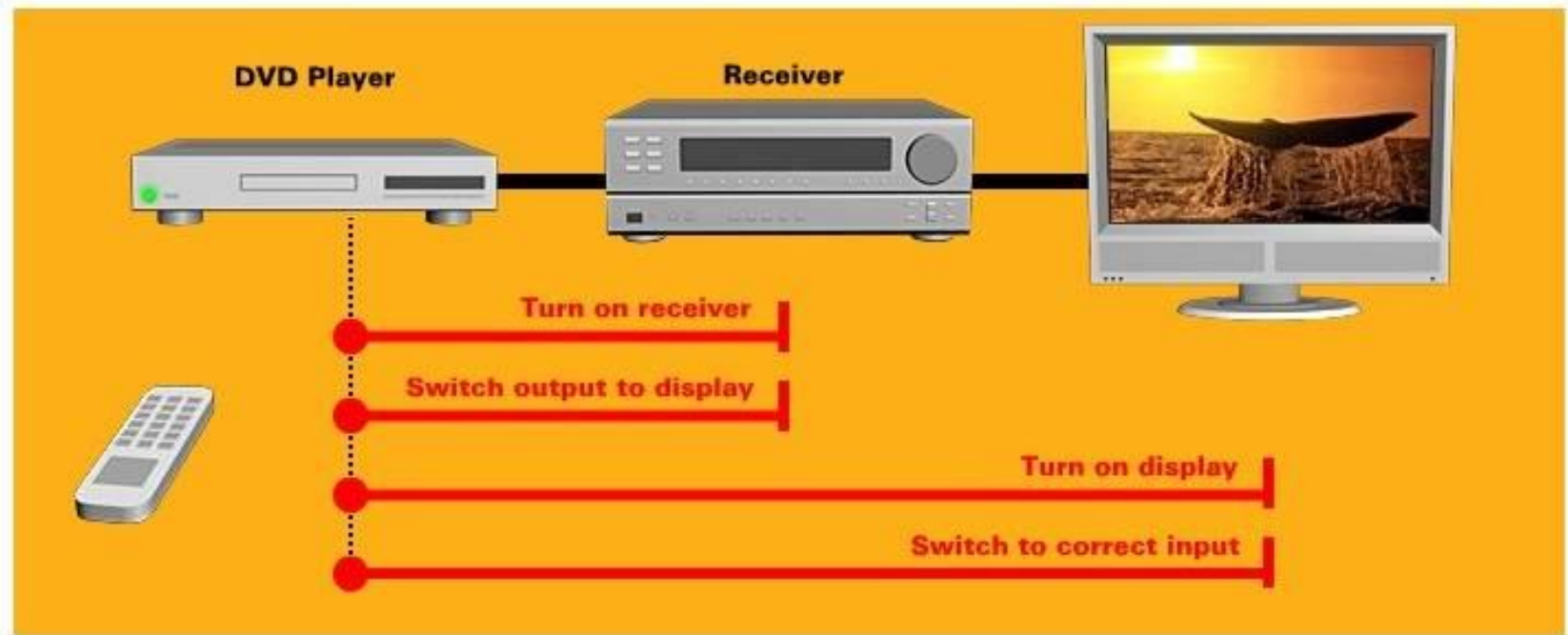
- Optional CEC Channel

- Carries device control function between all connected HDMI A/V devices
- Included v1.2a



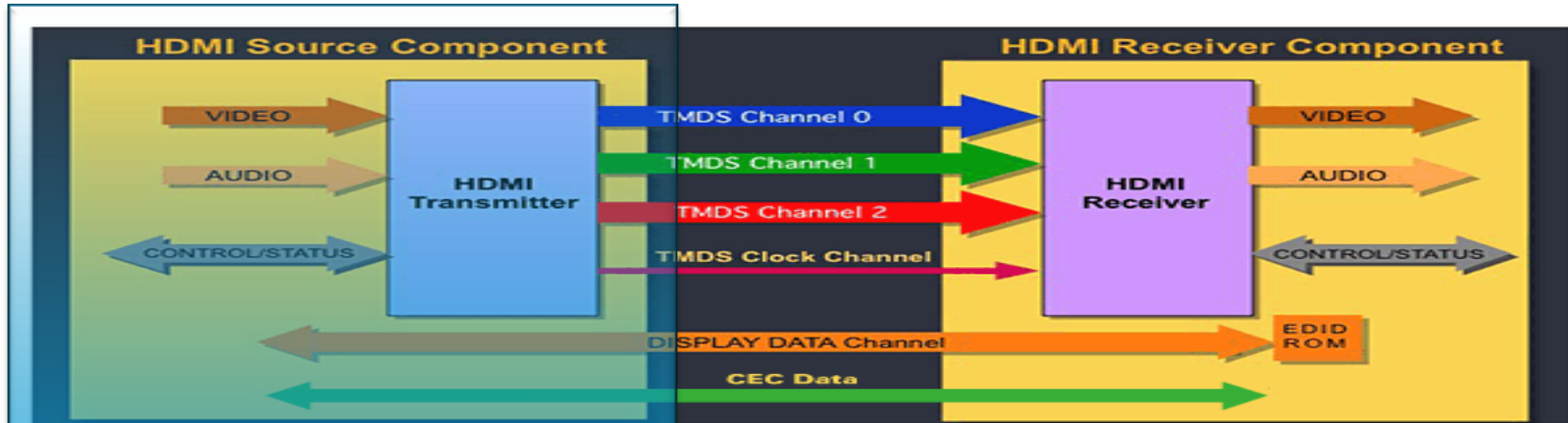
CEC (Consumer Electronic Control) (cont'd)

- Bi-directional serial bus
- Optional feature



Physical Layer Compliance Testing(1.4)

Source Testing



Source

- 7-4 : Rise/Fall Time
- 7-6 : Inter-pair Skew
- 7-8 : Clock Duty Cycle
- 7-9 : Clock Jitter
- 7-10 : Eye Diagram

Differential

- 7-2 : Voltage VL
- 7-7 : Inter-pair Skew

Single-ended

High Speed Electrical (TMDS) Source Test Solution

Required Tests

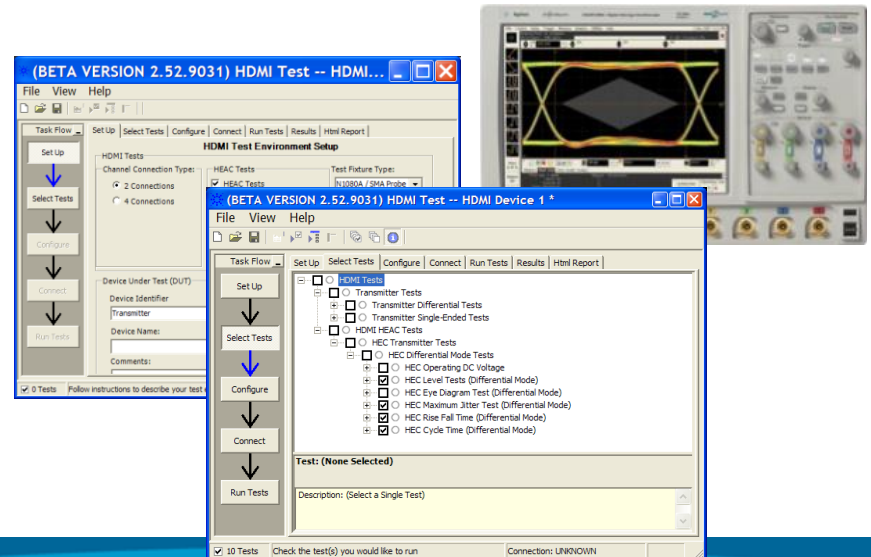
- Low voltage, rise & fall times, overshoot/undershoot, inter-pair skew, intra-pair skew, clock duty cycle, clock jitter, data eye diagram

Recommended Test Equipment

- **Realtime oscilloscope** DSO/DSA 9000A series 8GHz (DSO90804A) or higher
- Remote Programming Opt. 011 (if used with N5990A Test Automation S/W)
- **Probe Amplifier** 1169A (min. qty. 2, recommended 4)
- **SMA Probe Head** N5380A (recommended) or E2695A; min. qty. 2, recomm. 5
- **Compliance SW** N5399A Upgrade

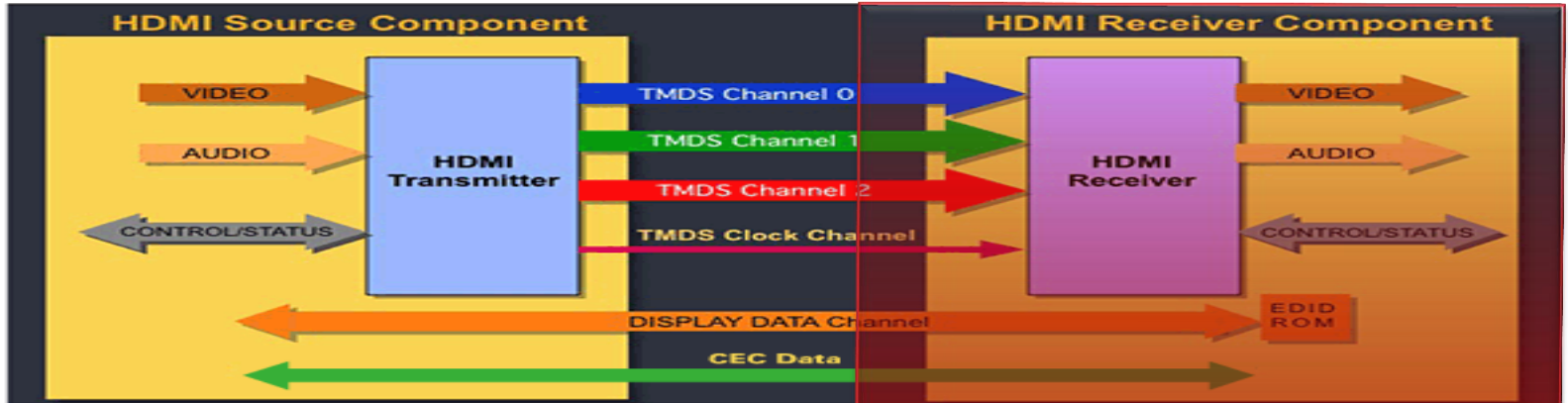
Agilent Value

- Accurate and repeatable results through lowers noise and probing systems
- Ease of use through Test Automation Software



Physical Layer Compliance Testing(1.4)

Sink Testing

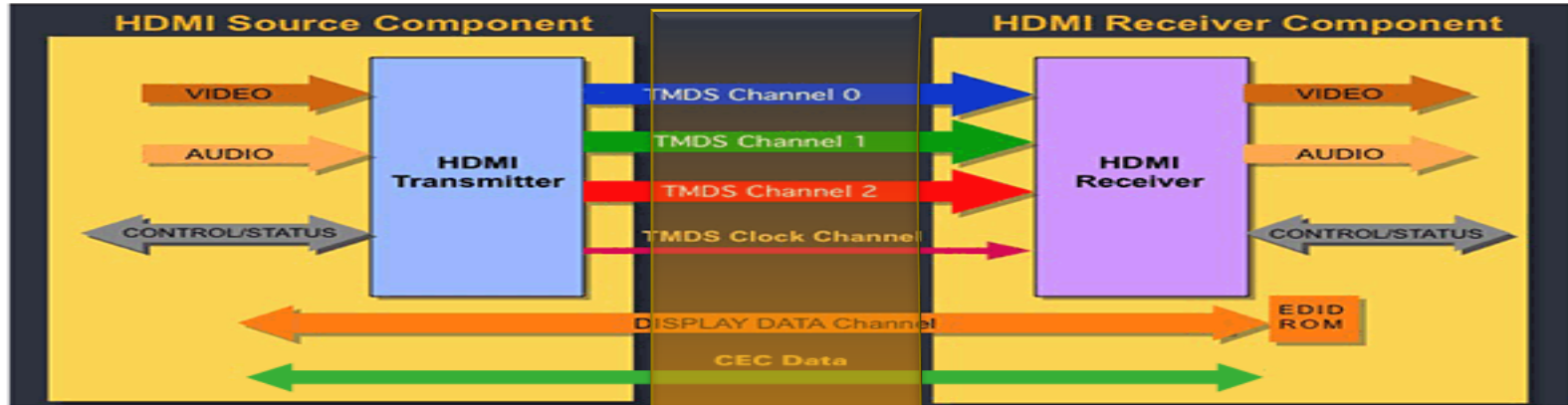


Sink

- 8-7 : Jitter Tolerance
- 8-5 : Min Differential Swing
- 8-6 : Inter-Pair Skew
- 8-8 : Differential Impedance

Physical Layer Compliance Testing(1.4)

Cable Test



Cable

- 5-3 : TMDS Data Eye Diagram
- 5-4,5-5 : Inter-pair and intra-pair Skew
- 5-8 : Diff. Impedance
- 5-6 : FEXT (Far End Crosstalk)
- 5-7 : Attenuation

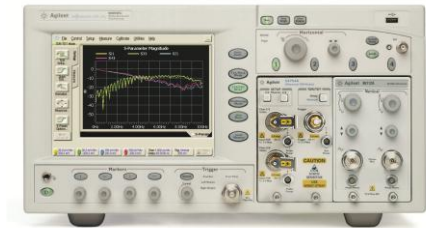
Cable Test Solution

Required Tests

- TMD5 data eye diagram, Intra-pair skew, Inter-pair skew, differential impedance, far-end crosstalk and Attenuation

Recommended Test Equipment

DCA-J	86100C
TDR module	54754A
Dual channel electrical receiver	86112A
ENA Series Network Analyzer	E5071C
Test Set, 9 kHz to 8.5 GHz	Option 480
4-port RF E-Cal module	E4431B

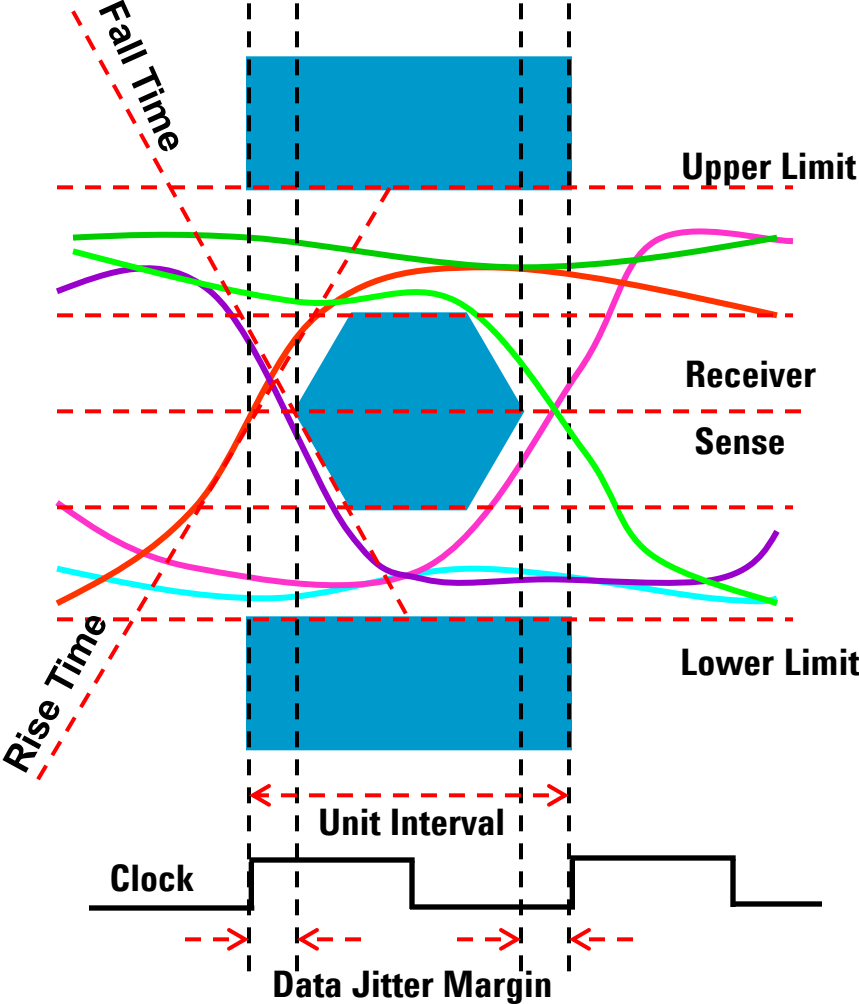


Agilent Value

- Characterize HDMI cables quickly and accurately

Source testing consideration

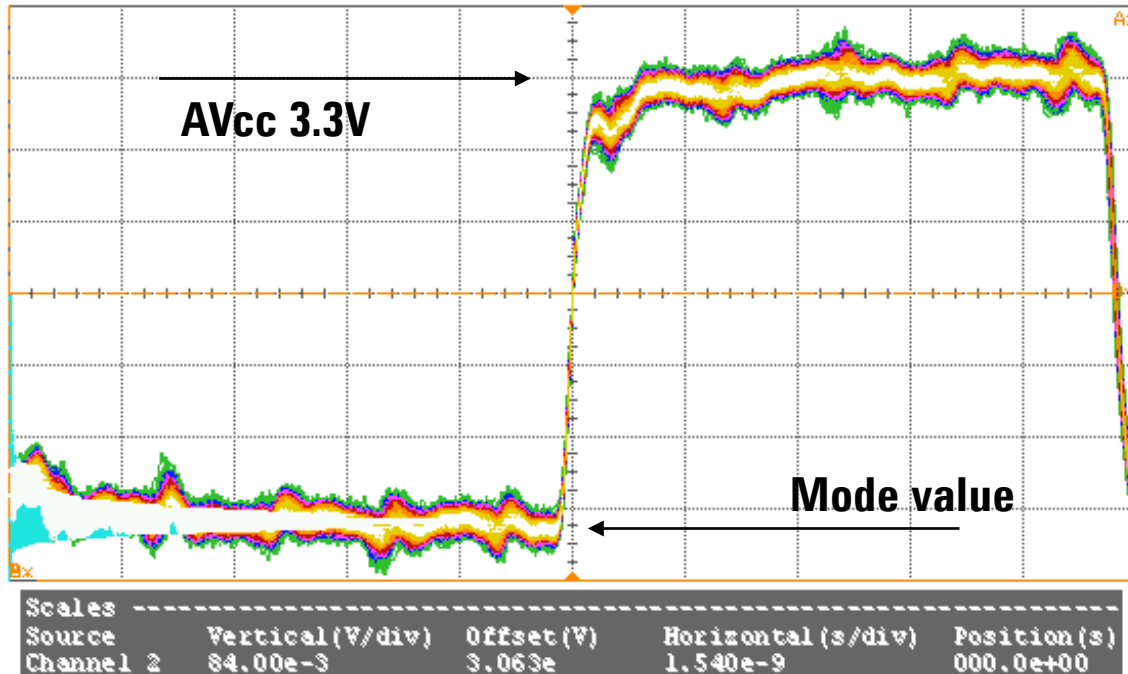
Eye pattern's Mask Test



Extracting of parameters

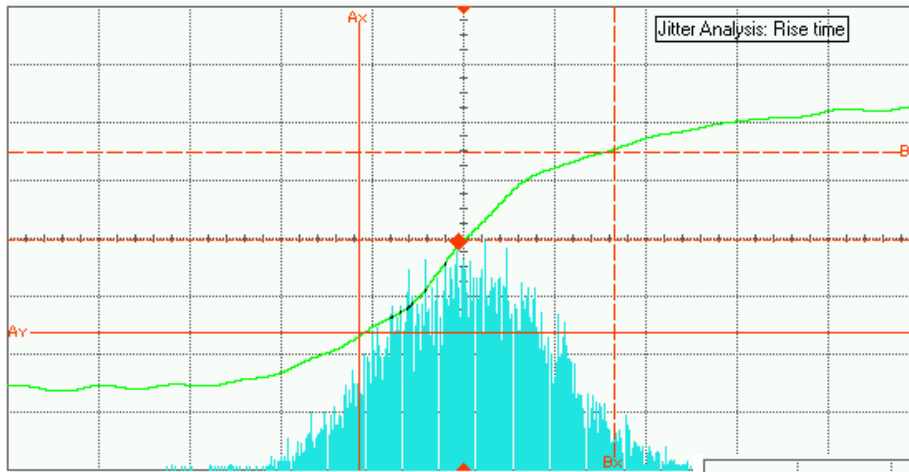
- VL
- Tr/Tf
- Intra-Pair skew
- Inter-Pair skew
- Clock Jitter
- Clock Duty Cycle
- Data Jitter

TestID 7-2 : VL

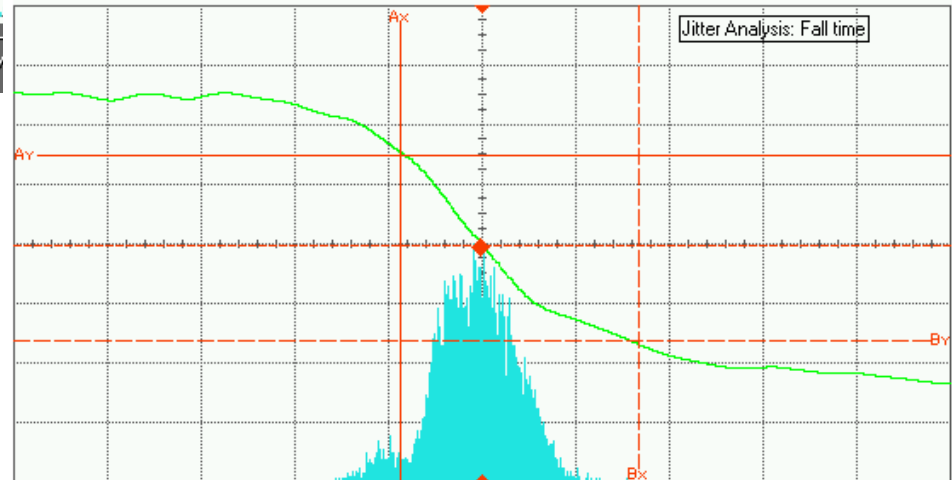


1. Pre calibration required on 50ohm termination part as 3.3V(Avcc)
2. Accumulating waveform with edge triggering
(In CTS1.4, it required to trigger H-L-L-L or L-H-H-H pattern for VL testing)
3. Measuring Histogram's mode value of vertical side(voltage)
4. Testing all single-end lines(D0+,D0-, ... CLK+, CLK-)

TestID 7-4 : Transition Time – Tr/Tf



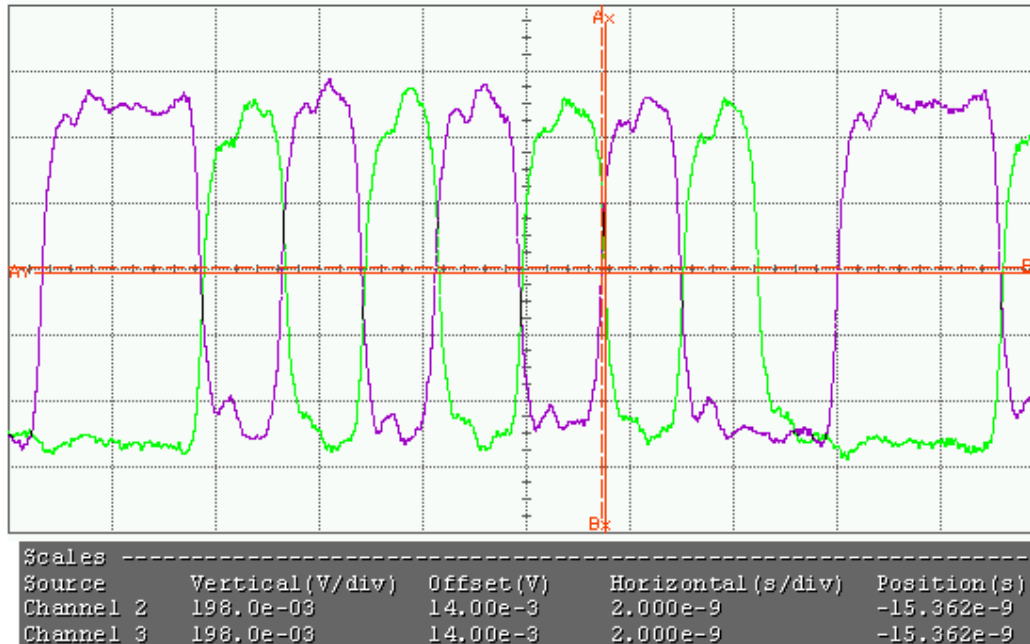
Source	Vertical (V/div)	Offset (V)	Horizontal (s/div)
Channel 2	198.0e-03	14.00e-3	108.0e-12



Source	Vertical (V/div)	Offset (V)	Horizontal (s/div)	Position (s)
Channel 2	198.0e-03	14.00e-3	108.0e-12	000.0e+00

1. Measure all of edges which Oscilloscope acquiring, and report mode value of histogram
2. Testing all differential lines (D0, D1, D2, CLK)

TestID 7-6 : Inter-Pair Skew



1. **With Pattern trigger, TMDS Sync pattern trigger**
2. **Check Sync pattern was acquired between 2 data lines**
3. **Measure acquired all bits' Delta time**
4. **Testing all differential DATA signals (D0, D1, D2)**

TestID 7-6 : Inter-Pair Skew

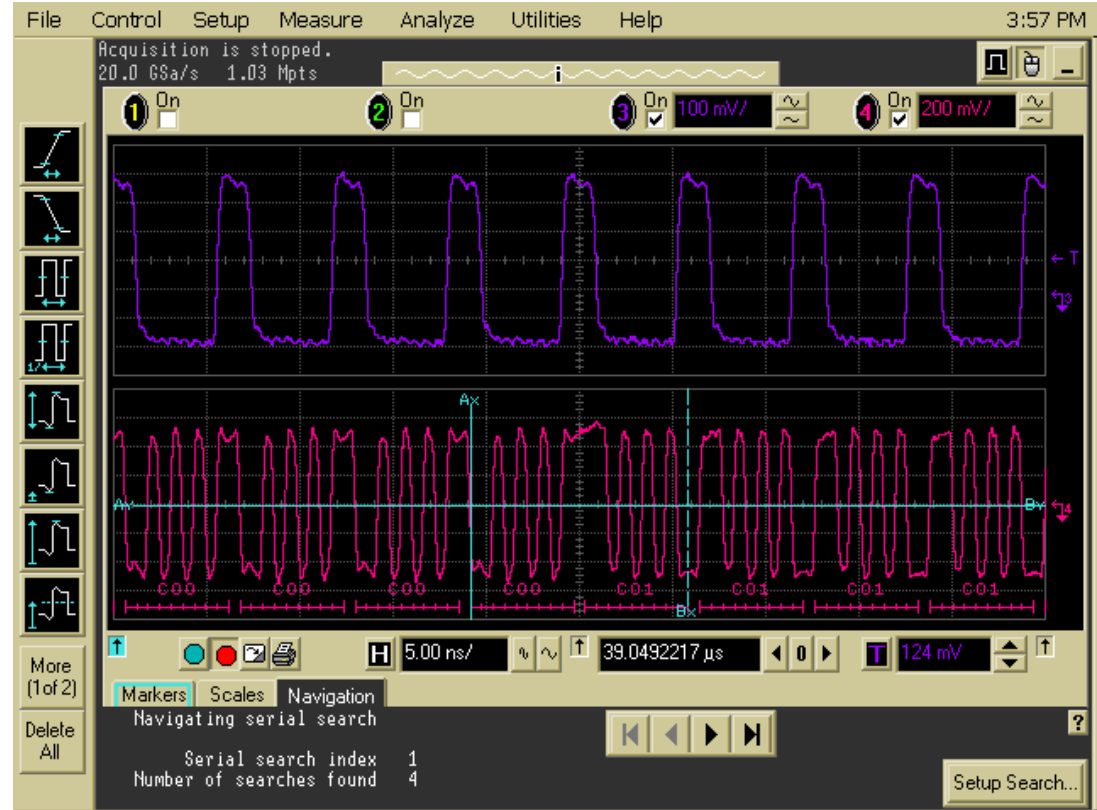
What is Sync pattern ?

Encoded Control signal

D1	D0	Sync Pattern [LSB:MSB]
0	0	0010101011
0	1	1101010100
1	0	0010101010
1	1	1101010101

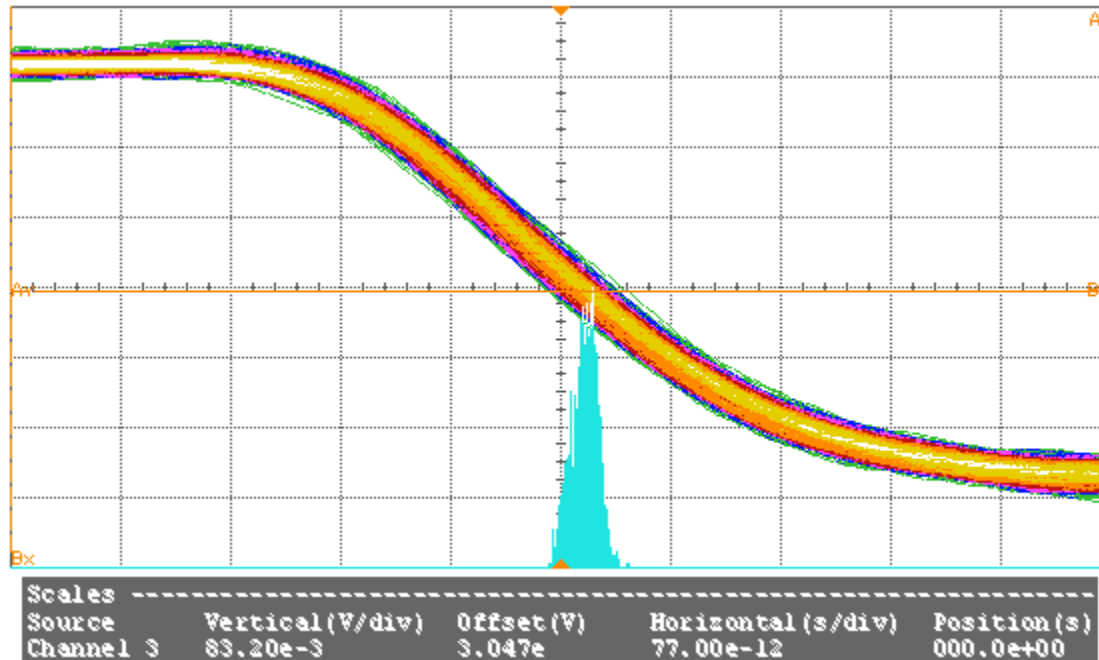
Control signal Assingment

TMDs Channel	D1	D0
0	VSYNC	HSYNC
1	CTL1	CTL0
2	CTL3	CTL2



An example of searching Sync pattern with E2688A HS-SDA software

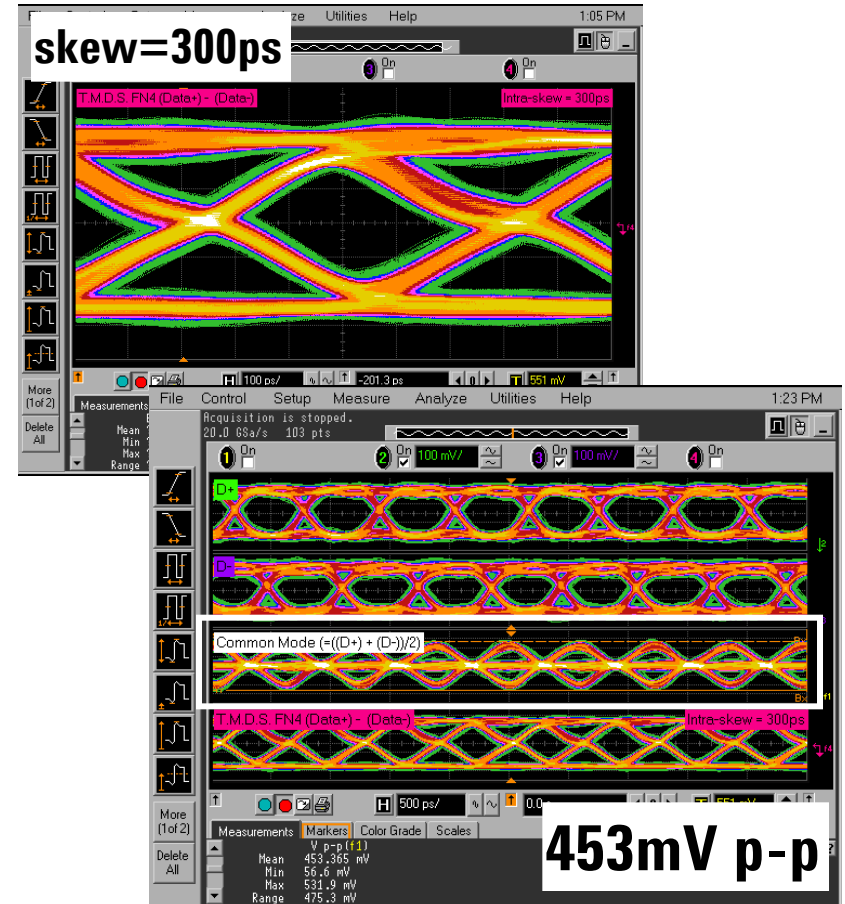
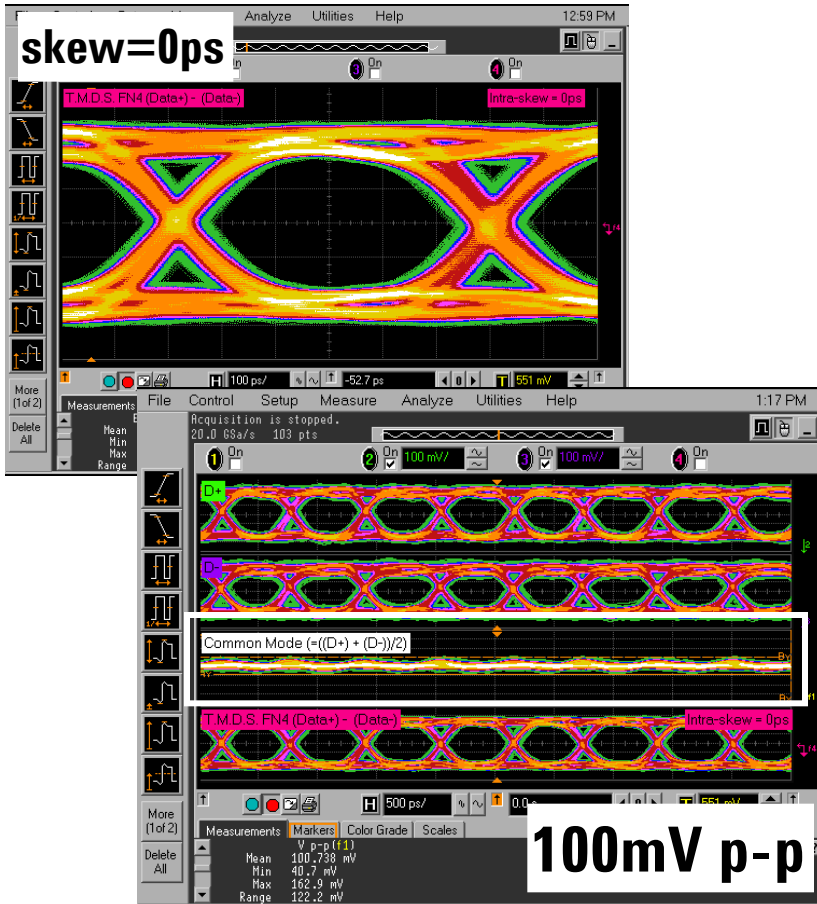
TestID 7-7 : Intra-Pair Skew



1. **Triggering on TMD5 positive(+) signal's rising edge**
2. **Measuring falling edges TMD5 negative(-) signal with histogram**
3. **Testing all differential pairs (D0+/-, D1+/-, D2+/-, CLK+/-)**

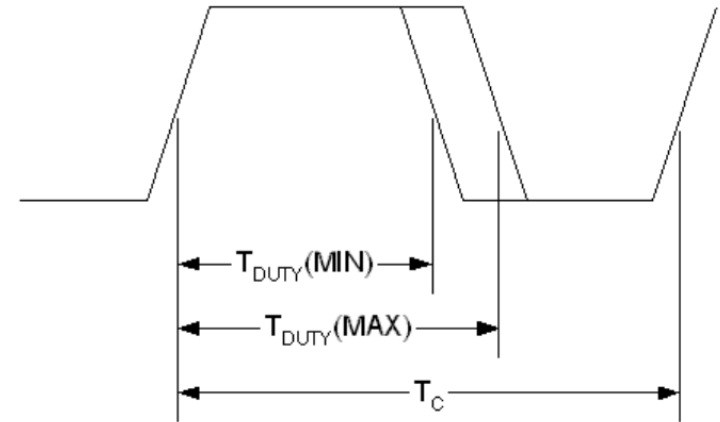
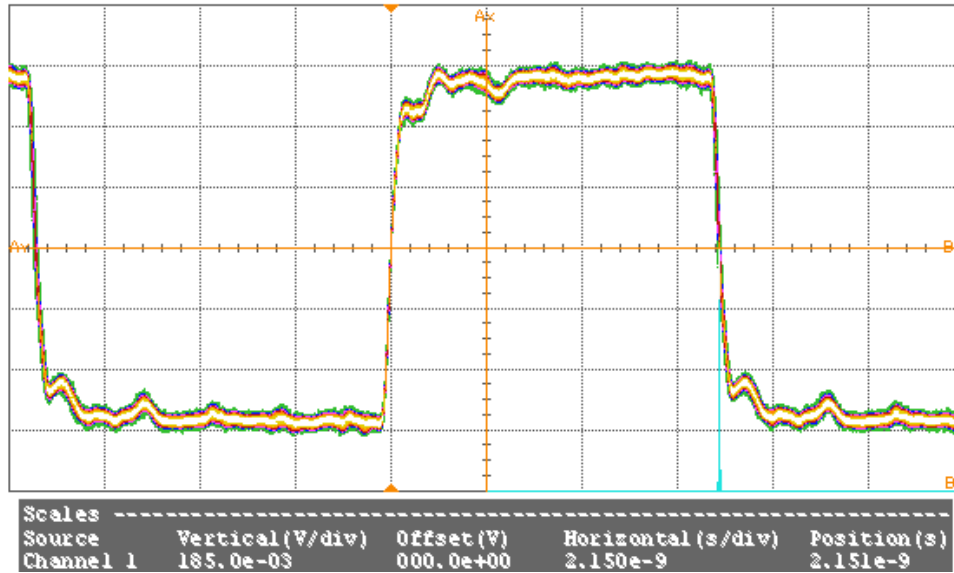
TestID 7-7 : Intra-Pair Skew

Effects of differential signal pair skew



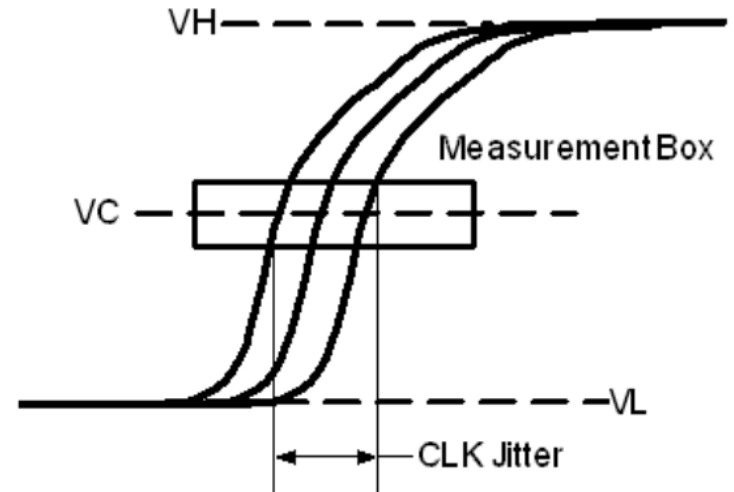
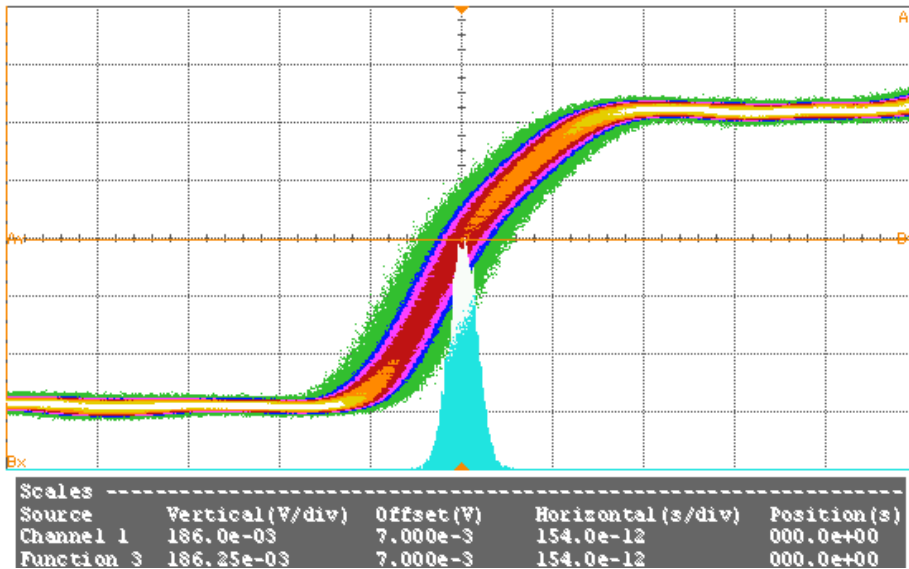
Waveform Distortion / Common mode noise increase

TestID 7-8 : Clock Duty Cycle



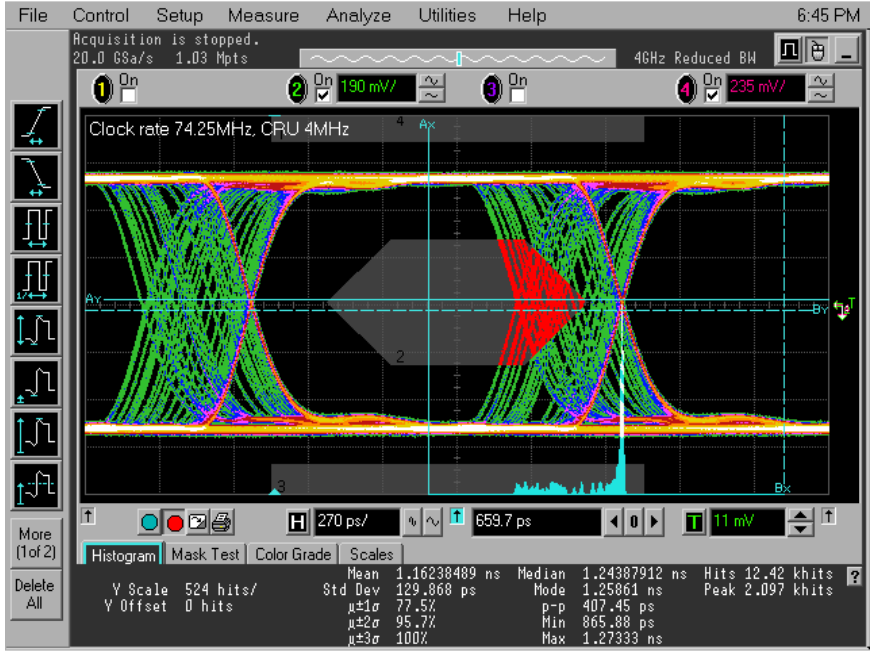
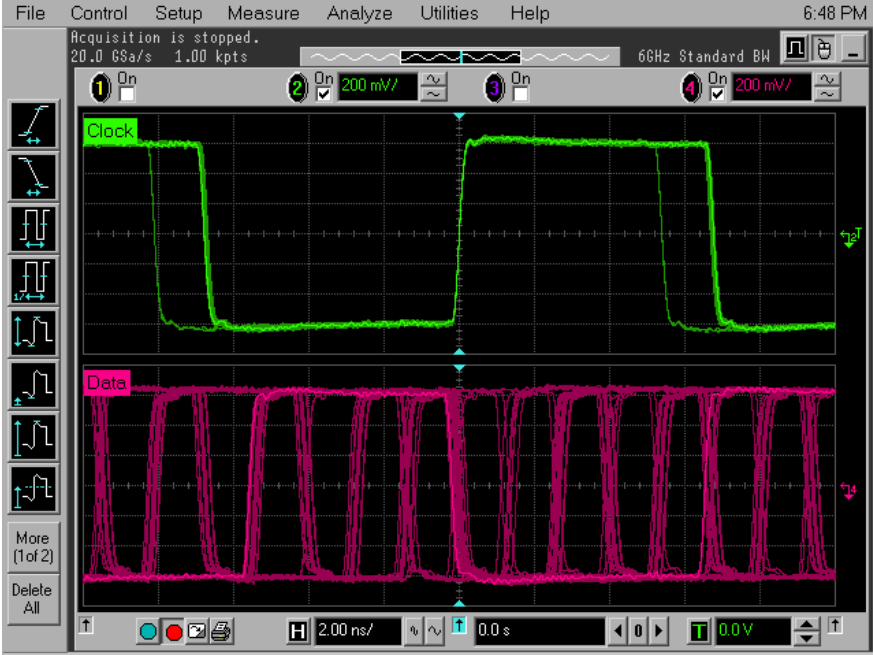
1. **Triggering TMD5 Clock rising edge**
2. **Measuring minimum and maximum duty cycle**

TestID 7-9 : Clock Jitter



1. **Triggering with software CRU's recovered clock**
2. **Measuring histogram at the point of edge ($0V \pm 20mV$)**

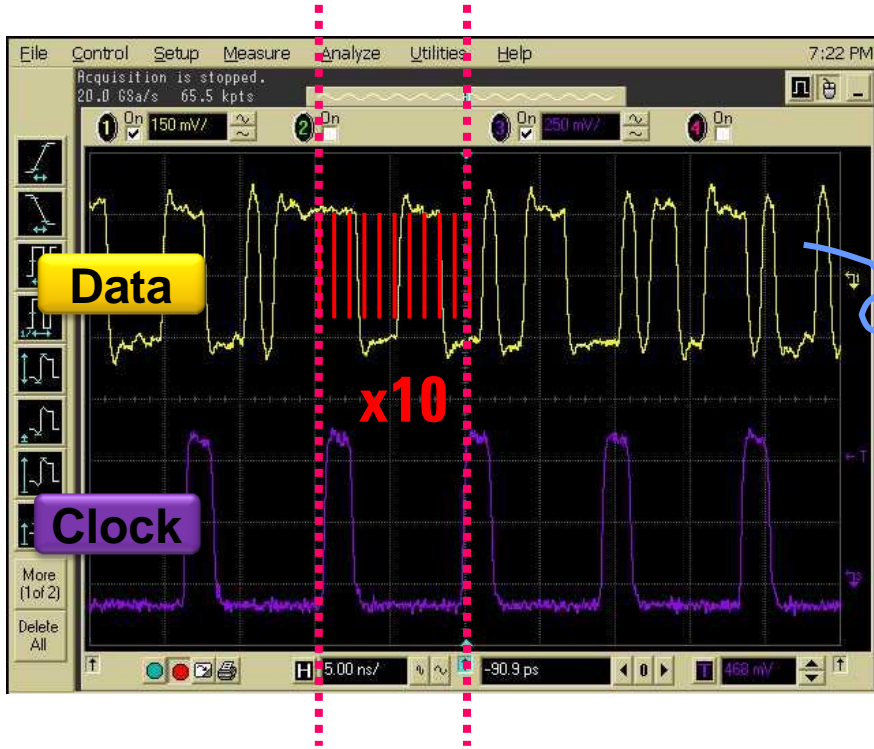
TestID 7-8, 7-9 Clock related items



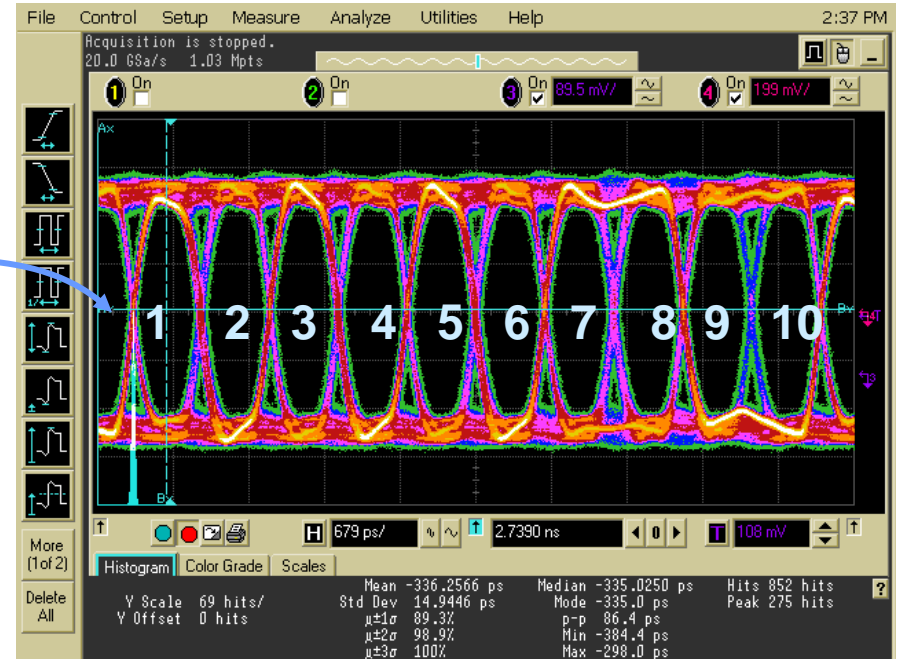
If clock is NOT stable, it will directly effect to DATA

TestID 7-9 : Data Eye Pattern

Clock and Data in HDMI



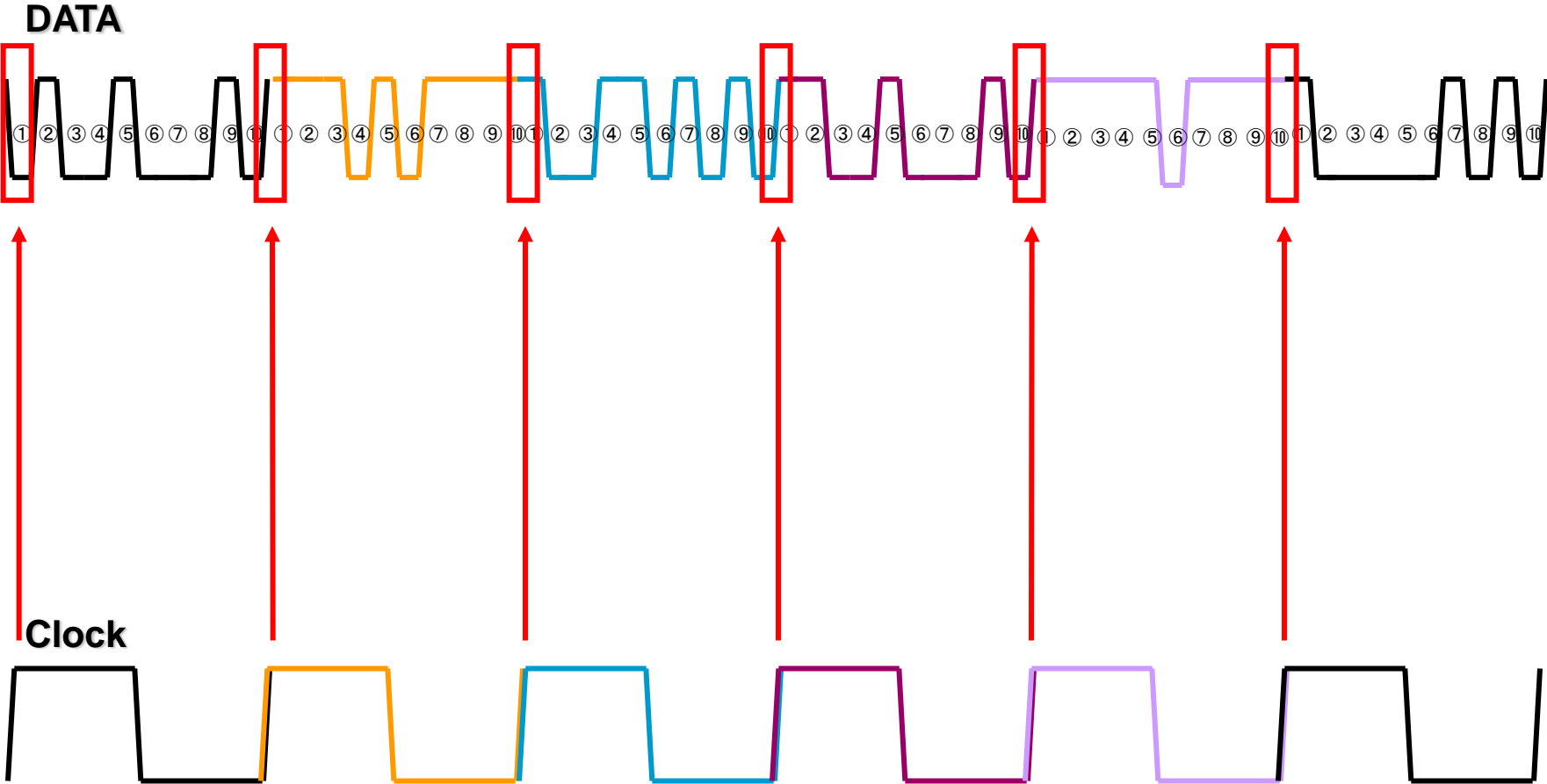
10 eye patterns of one clock period



- Clock signal is reference of data signal
- During 1 clock period, 10 TMDs unique eyes exist

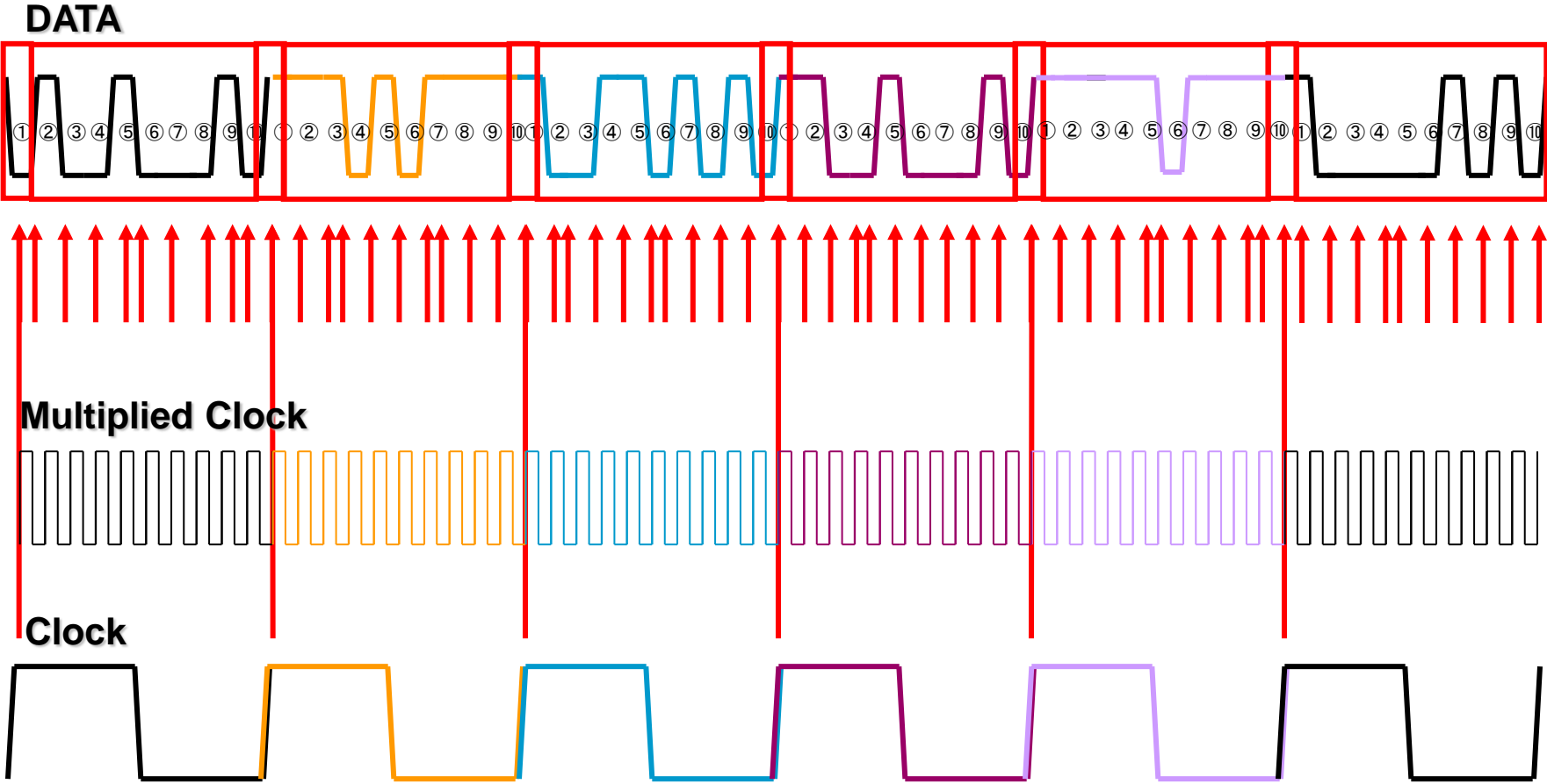
We can't guess signal quality with one eye like other application

Eye diagram with original method



Measure only first bit's eye diagram of 10 bits, Impossible to do TIE measurement

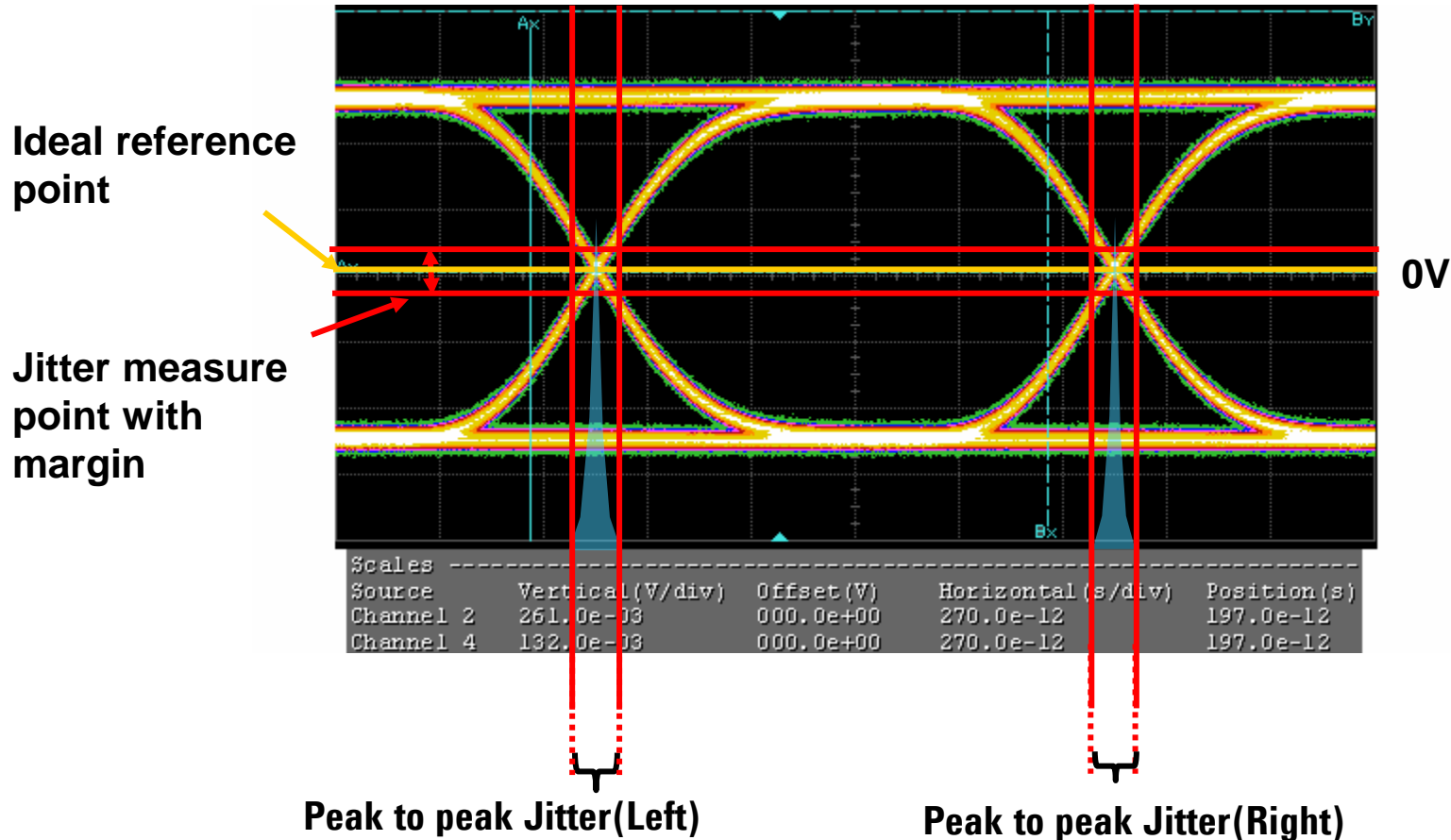
Eye diagram with multiplied clock method



Enabling measure all bit's eye diagram, TIE measurement

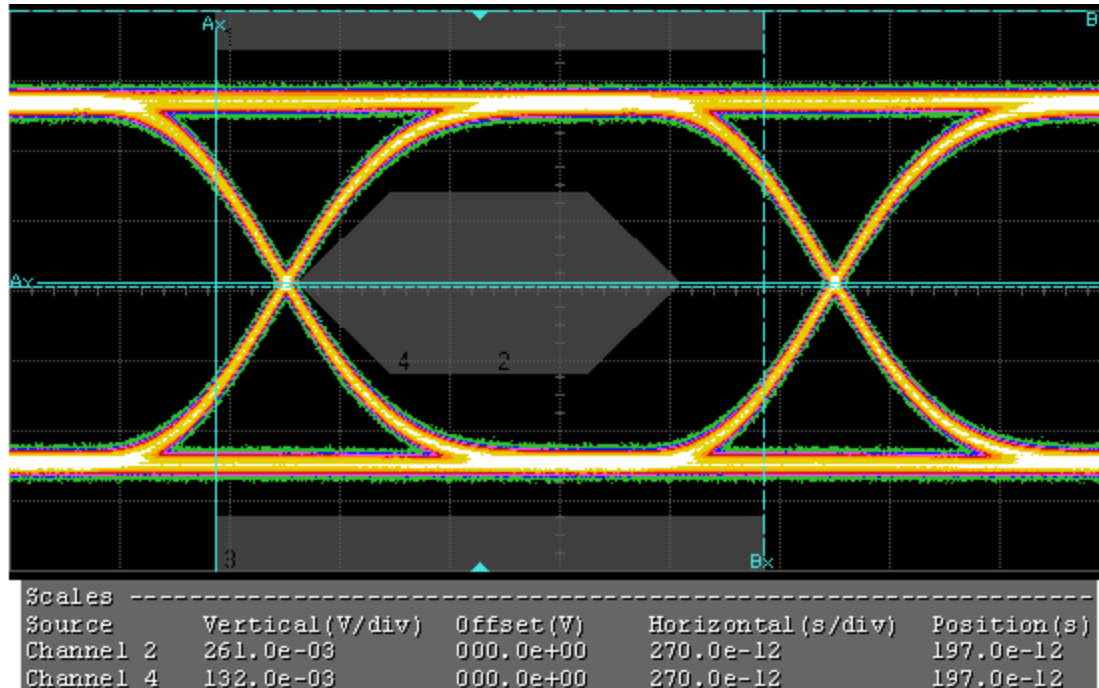
Multiplied eye diagram

Eye Diagram and Jitter measurement



Easily measure J p-p through Histogram in Oscilloscope

TestID 7-9 : Data Eye Pattern



1. **Align mask's X-axis(time) and Y-axis(volt)**
2. **Locate mask at 0V as center of Mask**
3. **Moving mask to left side until left edge of mask hit the signal**
4. **Check other point doesn't hit the signal**

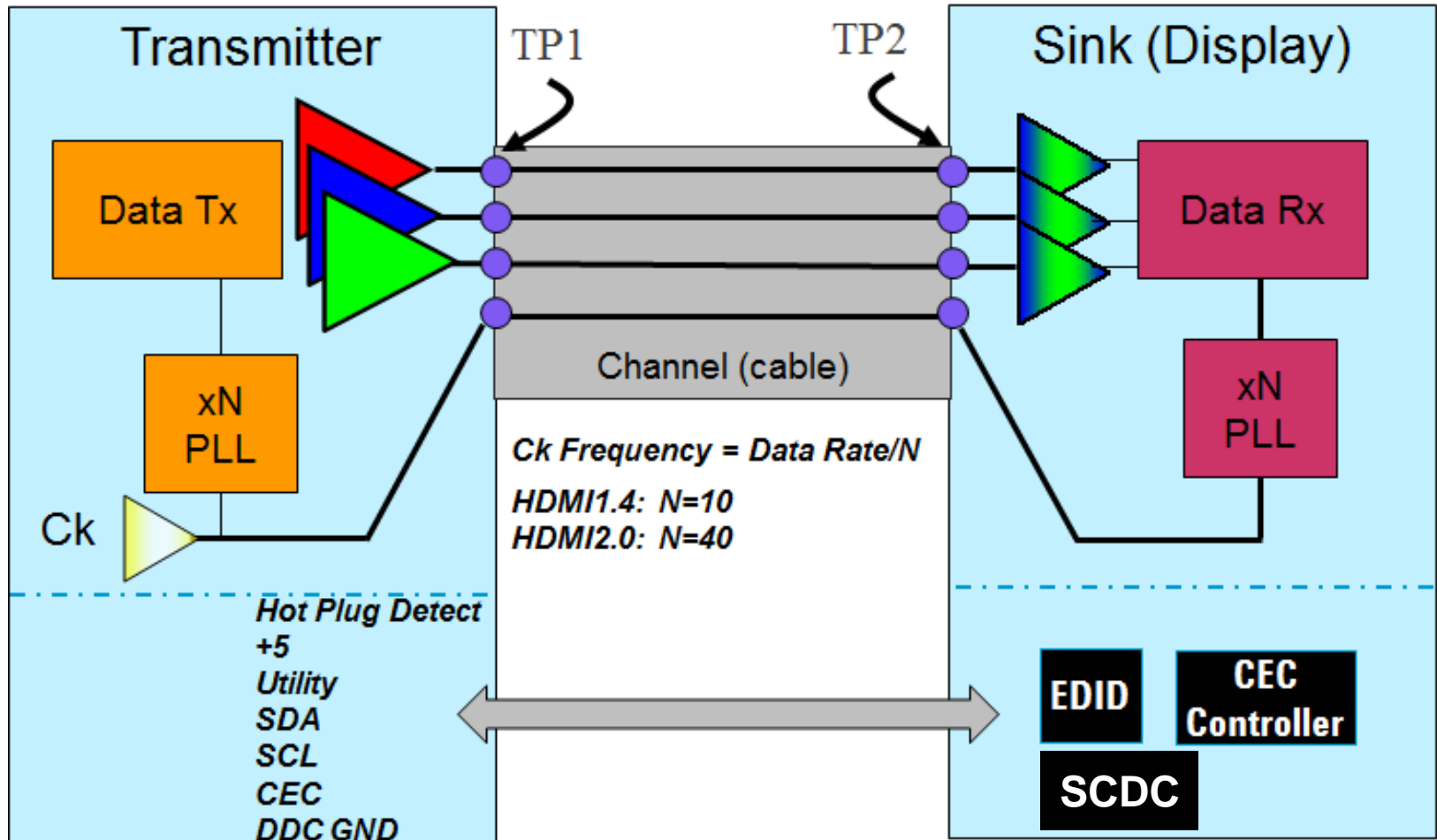
HDMI 2.0

Objectives of 2.0

- Increase the TMDS data rate to 6 Gbps
- Add Dual View mode
- Add a Direct Attach mode
- Add a Status Control and Data Channel (SCDC)
 - Scrambling for EMI/RFI reduction
- Add protocol testing for 4:2:0 4k2k 50/60 Hz (2.97 Gbps)
- Add some protocol layer enhancements (3D, etc)

- There are two specifications and two organizations in HDMI.
 - For HDMI 2.0: HDMI Forum with more than 80 member companies
 - For HDMI 1.4: HDMI.org led by 7 companies

HDMI Physical Interface



	Single lane Data Rate	Clock Freq	/N	Scrambling (SCDC)
HDMI 1.4	250M to 3.4Gbs	25M to 340MHz	10	No
HDMI 2.0	3.4-6.0Gbs	80.5 to 149.25	40	Yes

Physical Layer Test Details

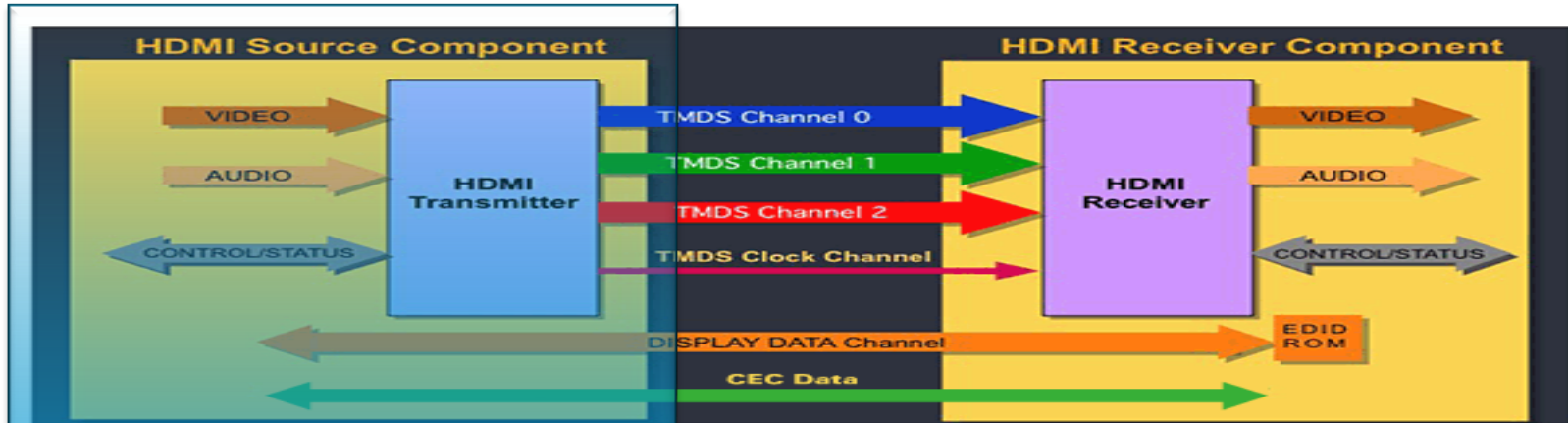
- HDMI 2.0 includes a 3.4 Gbps to 6 Gbps data rate band specification.
The new HDMI 2.0 Tx tests are called HF1-xx (Rx: HF2-xx)
The HDMI 1.4b Tx tests are TMDS 7-xx (Rx: 8-xx).
- For source testing, both sets of tests are selectable at the same time.

- Fixture De Embedding may be required. To be determined
- Channel Embedding required on a TP1 acquisition=>TP2
- HDMI 2.0 Equalization construct provided=>TP2EQ.
- Additional channel skew of 112ps added to each side of the differential pair.

These Functions are for the Oscilloscope to do in math

Physical Layer Compliance Testing(2.0)

Source Testing



Source

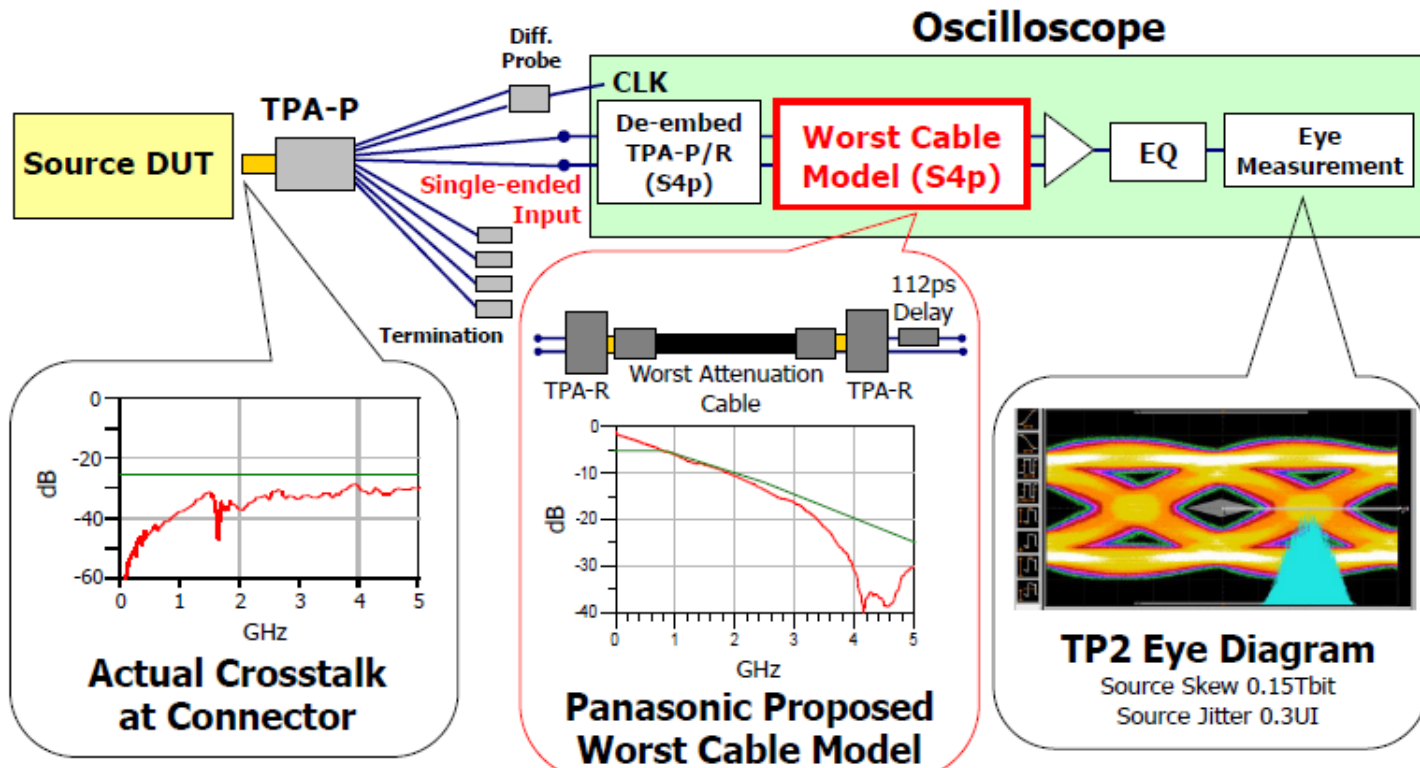
- **HF1-1 : V_L and V_{Swing}**
- **HF1-2 : T_{RISE} , T_{FALL}**
- **HF1-3 : Inter-pair Skew**
- **HF1-4 : Intra-pair Skew**
- **HF1-5 : Differential Voltage**
- **HF1-6 : Clock Duty and Rate**
- **HF1-7 : Clock Jitter**
- **HF1-8 : Eye Diagram**

Software Worst Case Cable Emulator for Tx Tests

HDMI Forum
Confidential

Source Data Eye Diagram Test Setup

- Proposed Worst Cable Model shall be embedded into Oscilloscope.
- Effect of Crosstalk, Cable Attenuation and Cable Skew can be reflected.



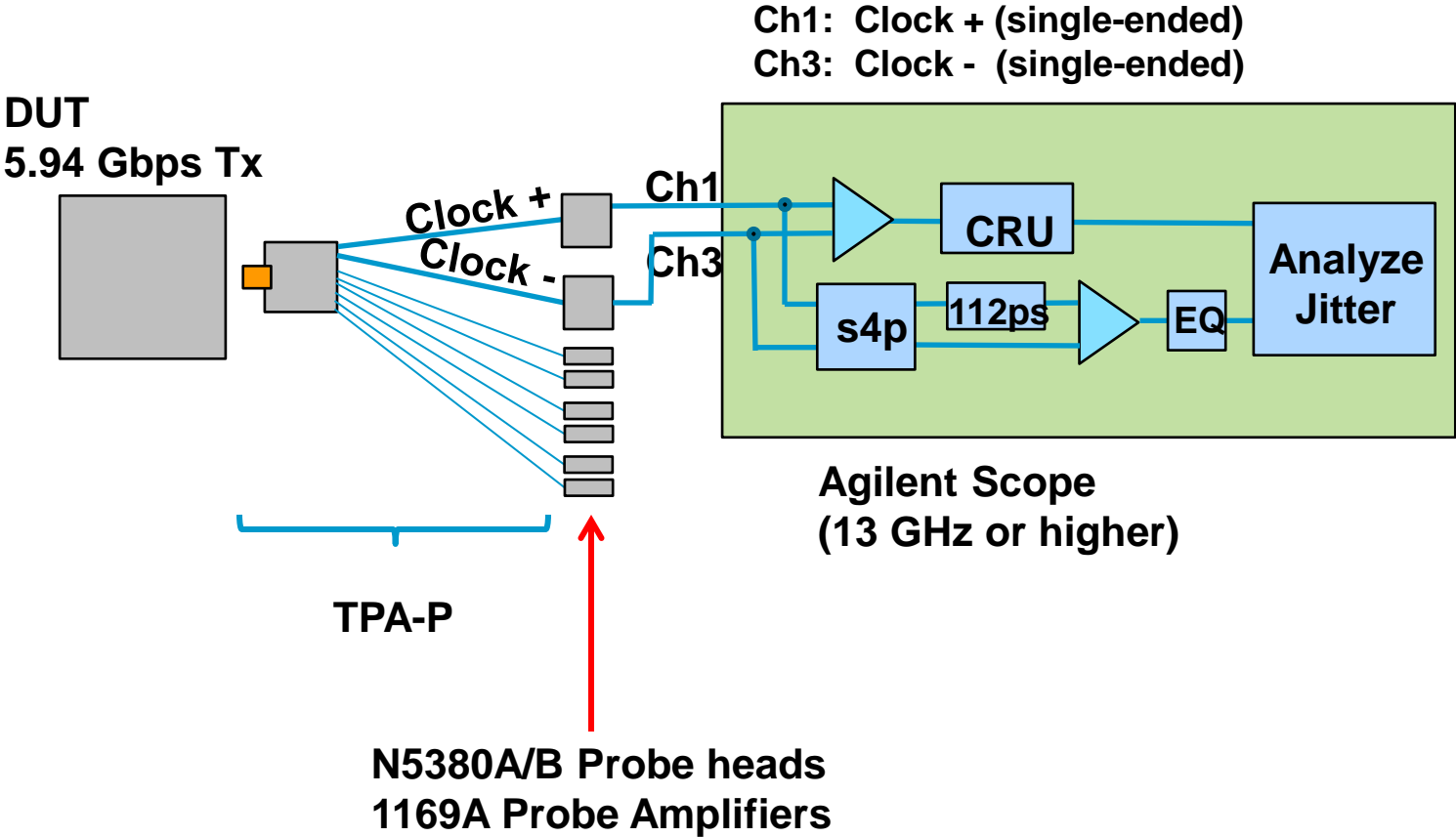
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3

Panasonic ideas for life

With permission from Panasonic

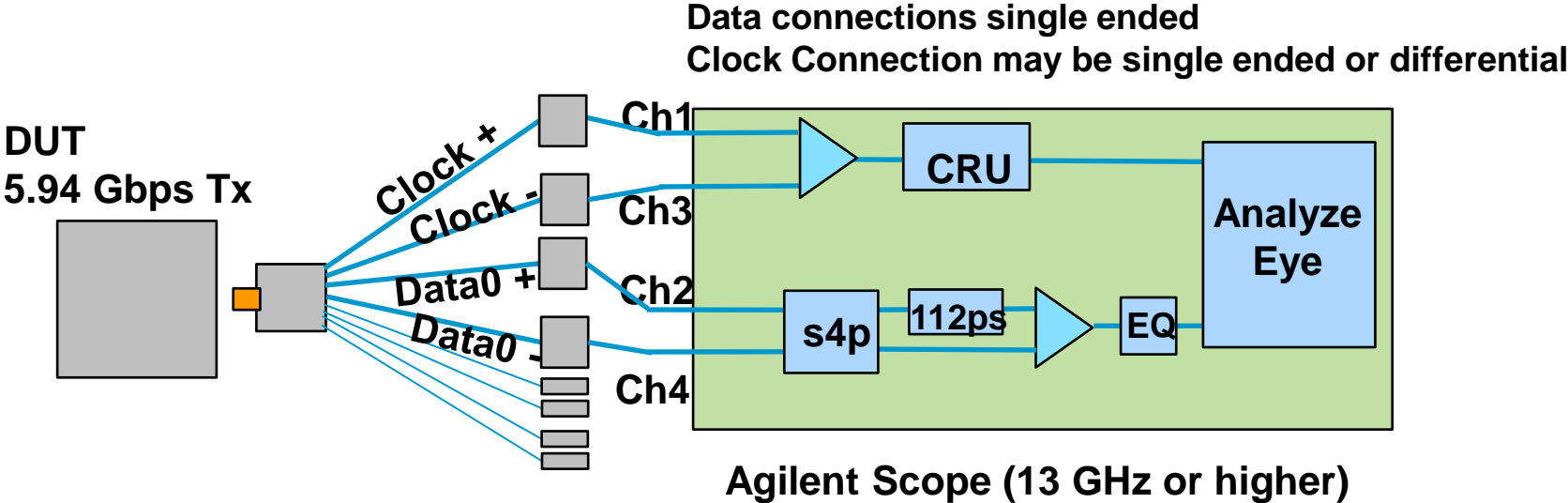
Tx Clock Jitter Measurement



+3.3V Pull up Termination for all channels TMD5 lanes

Test both cases of 112 ps delay in positive and negative sides

Tx Data Eye Measurement



TPA-P

TPA-P

N5380A/B Probe heads
1169A Probe Amplifiers

+3.3V Pull up Termination for
all channels TMD5 lanes

Test both cases of 112 ps delay
in positive and negative sides

Equalization in HDMI

Equalization is stipulated to follow the relation below for freq response.
Phase of equalizer must be manifest to yield causal filter with this response

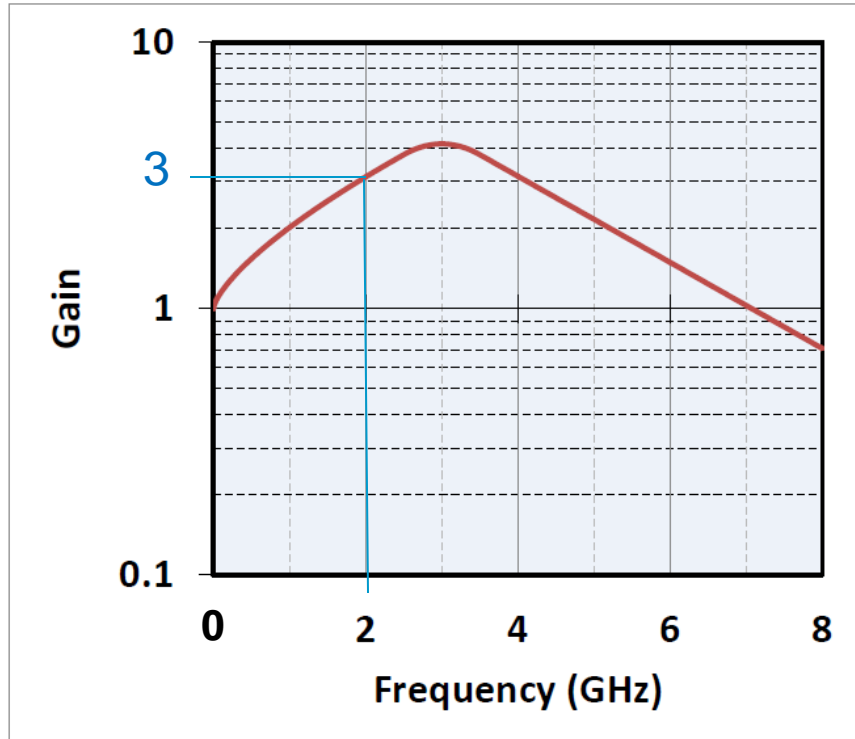


Figure 6-2: Reference Cable Equalizer for 3.4 Gbps < R_{bit} ≤ 6 Gbps

$$|H(j\omega)| = \begin{cases} e^{A*\omega^N} & (\omega < \omega_0) \\ e^{-B*(\omega-1.2*\omega_0)^2+C} & (\omega_0 < \omega < 1.4*\omega_0) \\ e^{-D*\omega+E} & (1.4*\omega_0 < \omega) \end{cases}$$

Where

$$N = 0.7$$

$$\omega_0 = 2\pi * 2.5\text{GHz}$$

$$A = 9.7E-8$$

$$B = \frac{7}{4} * A * \omega_0^{-1.3}$$

$$C = 1.07 * A * \omega_0^{0.7}$$

$$D = 0.7 * A * \omega_0^{-0.3}$$

$$E = 1.98 * A * \omega_0^{0.7}$$

Equation 6-2: Reference Equalizer Equations for 3.4 Gbps < R_{bit} ≤ 6.0 Gbps

HDMI Tx App Tour: Entry Screen

(BETA VERSION 1.99.9027) HDMI HEAC Test -- HDMI Device 1

File View Tools Help

Task Flow: Set Up | Select Tests | Configure | Connect | Run Tests | Automation | Results | Html Report

HDMI Test Environment Setup

HDMI Tests Compliance Mode Debug Mode

HDMI Specs
2.0

Test Suite
 TMD5 Physical Layer Tests
 HEAC Tests
 Direct Attach Tests

Device Definition
Device Definition Incomplete..

Connection Setup
Connection Setup Incomplete..

Transfer function generation
Transfer Functions Ready
Set up embed/de-embed

Probe Offset Calibration
Last Calibration Date:
[View Offset Calibration Value](#) Offset Enabled
Probe Offset Calibration

0 Tests | Follow instructions to describe your test environment | Connection: UNKNOWN

HDMI 2.0 Pixel Clock <165MHz

Device information

Timings to Test

Create/Store Testplan

Testplan Creation From:

- CDF
- Stored template
- PC LAN
- Manual automatic EDID control is possible.

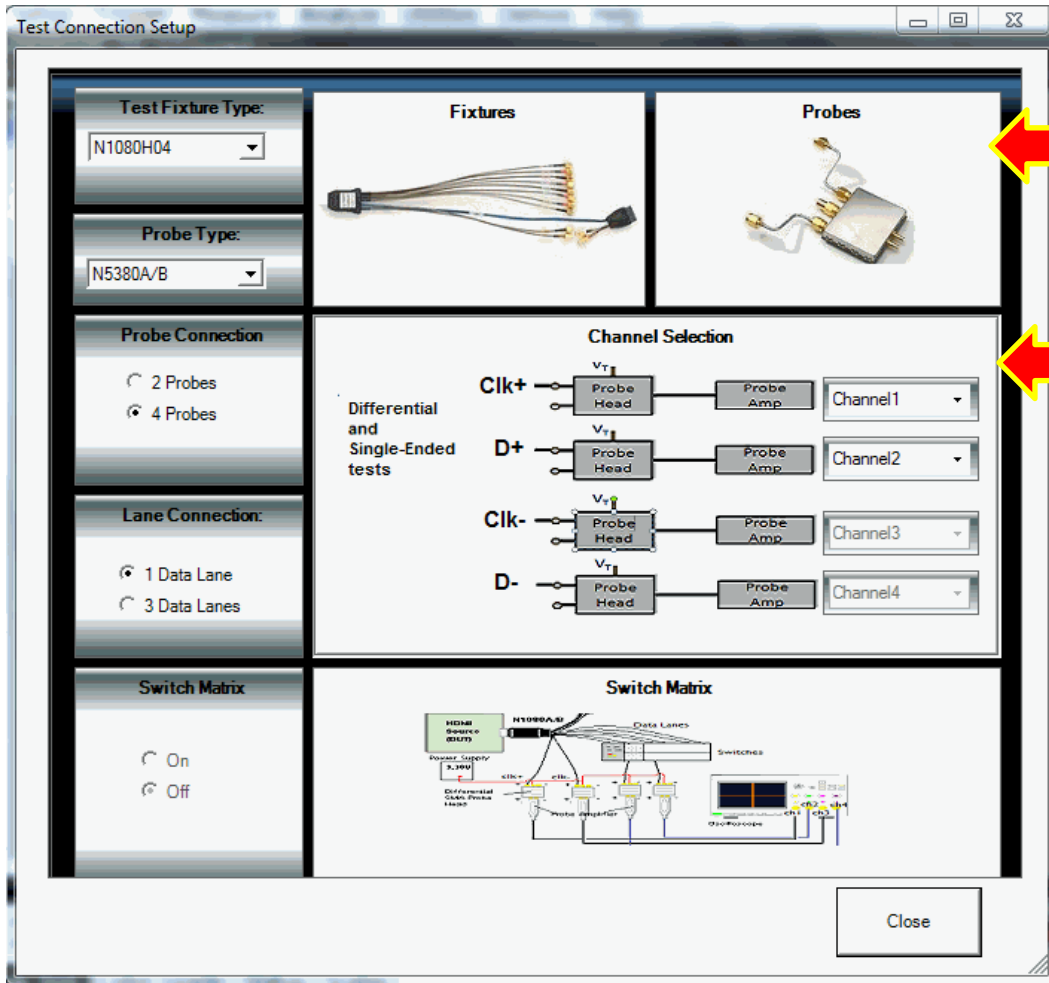


HDMI Tx App Tour: Entry Screen

The screenshot shows the 'HDMI HEAC Test -- HDMI Device 1' application window. The title bar indicates it is a BETA VERSION 1.99.9027. The menu bar includes File, View, Tools, and Help. The toolbar contains icons for file operations and navigation. The main interface is divided into several sections:

- Task Flow:** A vertical sidebar on the left with buttons for 'Set Up', 'Select Tests', 'Configure', 'Connect', and 'Run Tests'. A blue arrow points to 'Select Tests'.
- HDMI Test Environment Setup:** The main content area with tabs for 'Set Up', 'Select Tests', 'Configure', 'Connect', 'Run Tests', 'Automation', 'Results', and 'Html Report'.
 - HDMI Tests:** Includes 'HDMI Specs' (set to 2.0), 'Test Suite' (with radio buttons for 'TMDS Physical Layer Tests', 'HEAC Tests', and 'Direct Attach Tests'), and 'Device Definition' (with a 'Device Definition Completed' message and a red arrow pointing to it). Below it is 'Connection Setup' with a 'Connection Setup Incomplete..' message.
 - Transfer function generation:** Includes a 'Transfer Functions Ready' message and a 'Set up embed/de-embed' button.
 - Probe Offset Calibration:** Includes 'Last Calibration Date:', a 'View Offset Calibration Value' link, and a checked 'Offset Enabled' checkbox. Below it is a 'Probe Offset Calibration' button.
- Status Bar:** At the bottom, it shows '0 Tests', 'Follow instructions to describe your test environment', and 'Connection: UNKNOWN'.

Connection Setup



Probe Head and Fixture selection

Number and type of connection. Differential Vs Single ended.

4 probe/1 data lane is

4 SE channel connections

4 probe/3 data lanes is

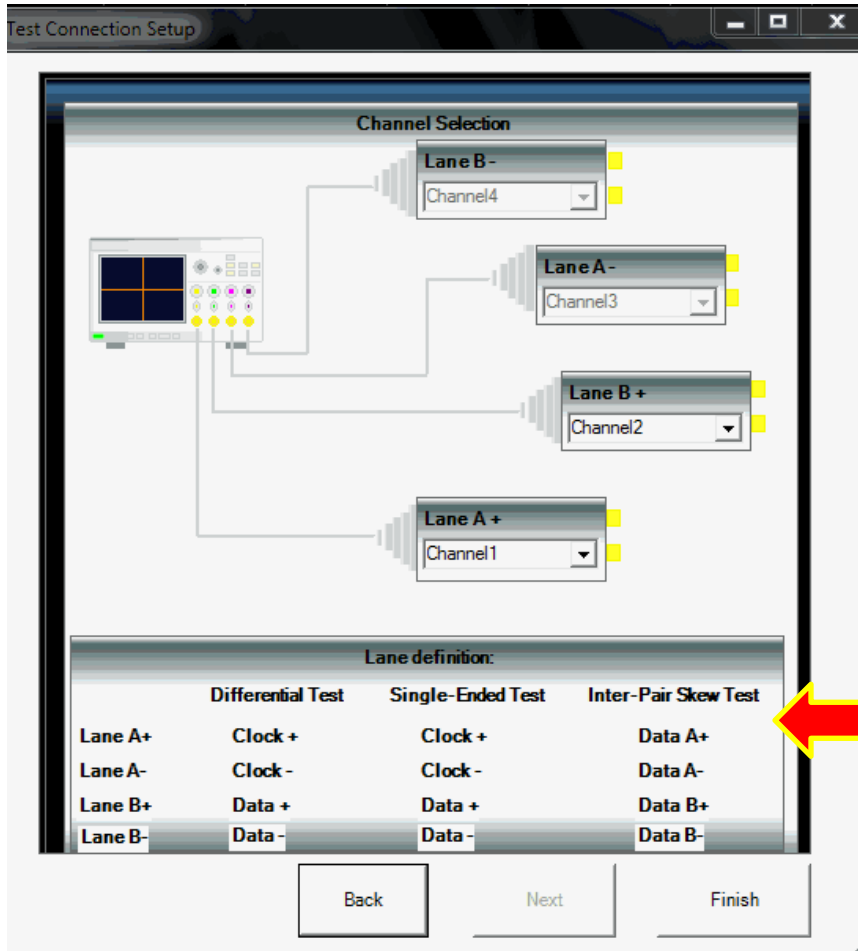
4 Diff connections

2 Probe/1 data lane is

2 Diff connections or

2 SE connections

Probe/Channel Assignments



This is a 4 channel/1 Data lane connection
In this configuration you can connect:

-clock+ /clock - for

single ended testing of the clock lane
differential testing of the clock

-data+/data-

single ended testing of the data lane
differential testing of the data lane

-dataA+/dataA- & dataB+/dataB- for:
interpair skew testing.

Entry Screen after completing setups

The screenshot displays the 'HDMI HEAC Test' software interface. The window title is '(BETA VERSION 1.99.9027) HDMI HEAC Test -- HDMI Device 1 *'. The menu bar includes 'File', 'View', 'Tools', and 'Help'. The main interface is divided into a 'Task Flow' sidebar on the left and a main content area. The 'Task Flow' sidebar shows a sequence of steps: 'Set Up', 'Select Tests', 'Configure', 'Connect', and 'Run Tests'. A blue arrow points to 'Set Up', and a red arrow points to the 'Connection Setup' button in the main content area.

The main content area is titled 'HDMI Test Environment Setup' and contains several sections:

- HDMI Tests**: Includes a dropdown menu for 'HDMI Specs' set to '2.0'.
- Test Suite**: Features radio buttons for 'Compliance Mode' (selected), 'Debug Mode', 'TMD5 Physical Layer Tests', 'HEAC Tests', and 'Direct Attach Tests'.
- Device Definition**: A button with the status 'Device Definition Completed' below it.
- Connection Setup**: A button with the status 'Connection Setup Completed' below it, highlighted by a red arrow.
- Transfer function generation**: Includes a button 'Set up embed/de-embed' and the status 'Transfer Functions Ready'.
- Probe Offset Calibration**: Includes a button 'Probe Offset Calibration', the status 'Last Calibration Date:', a link 'View Offset Calibration Value', and a checked checkbox for 'Offset Enabled'.

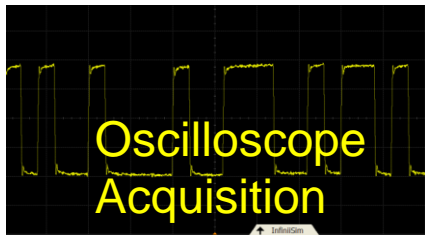
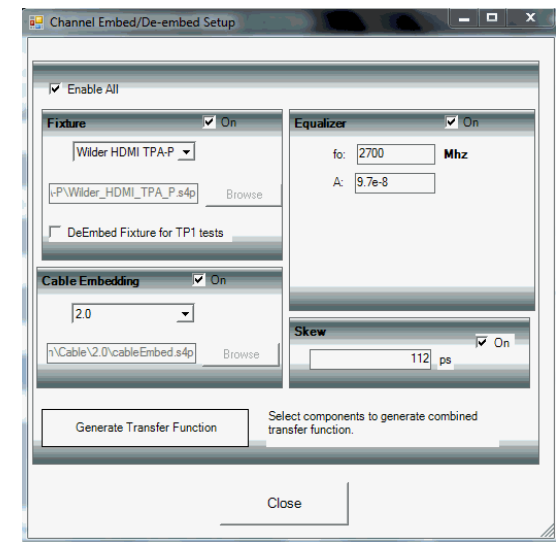
At the bottom of the interface, there is a status bar with the following information:

- 0 Tests
- Follow instructions to describe your test environment
- Connection: UNKNOWN

Transfer Function Generation

Required for the mathematical processes required in the specification:

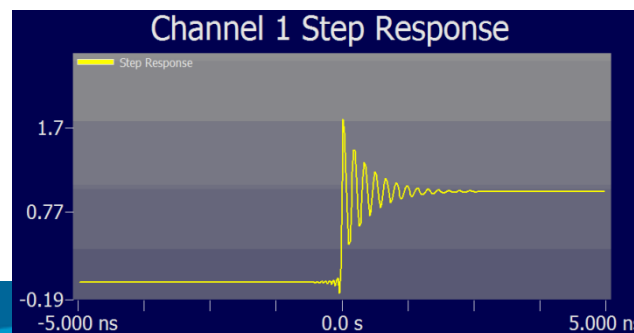
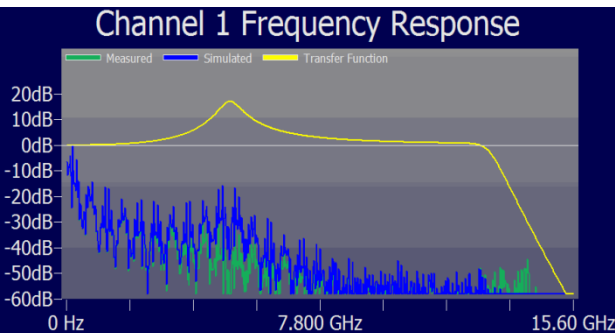
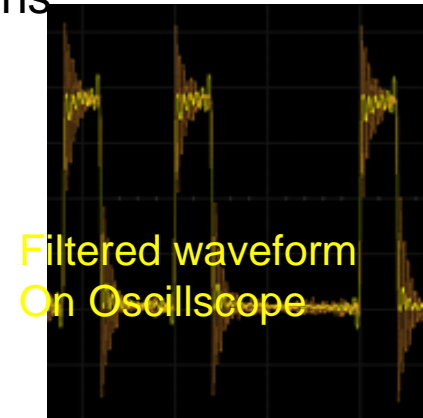
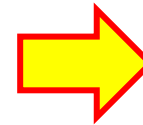
- ✓ embedding a cable
- ✓ de-embedding a fixture
- ✓ applying equalization
- ✓ skew setting
- ✓ transition time converter filtering
- ✓ The N5399C allows user to create arbitrary transfer functions



Time Domain 'Filter'



Frequency Domain Description



Transfer Function Generation

Fixture de embedding

- Agilent
- Wilder
- Bitifeye
- custom



Cable embedding

- standard HDMI 2.0
- custom

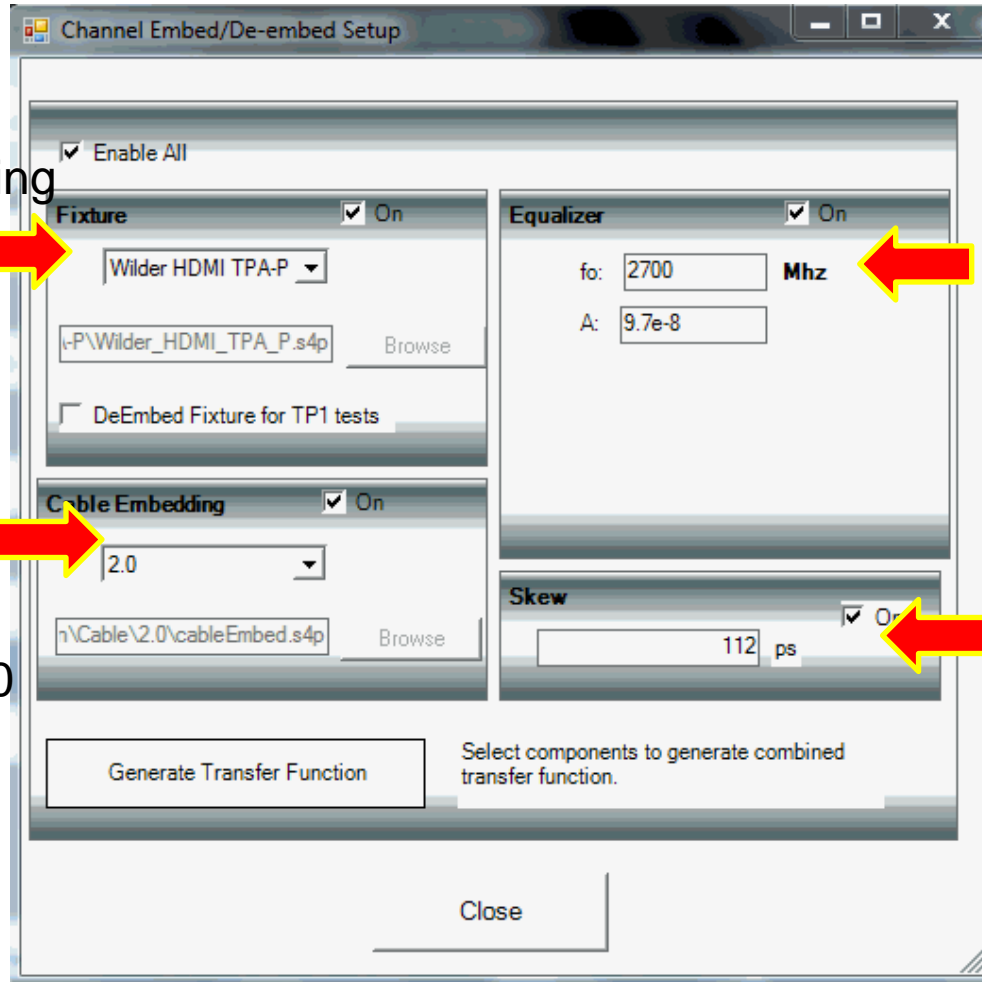


Equalizer Function

- HDMI 2.0
- CTLE
- custom

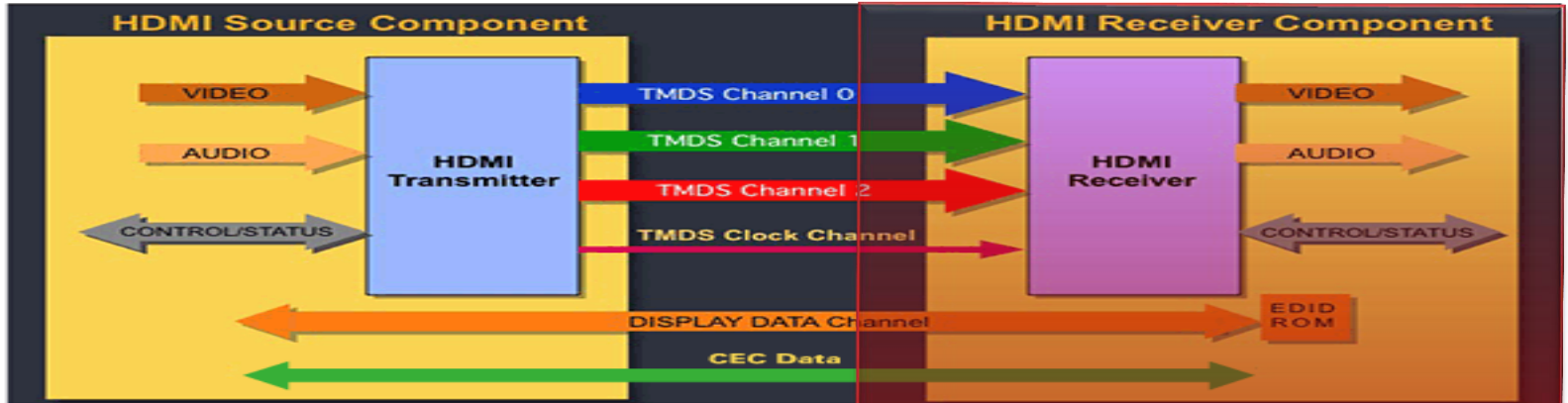


Additional Skew (lumped)



Physical Layer Compliance Testing(2.0)

Sink Testing

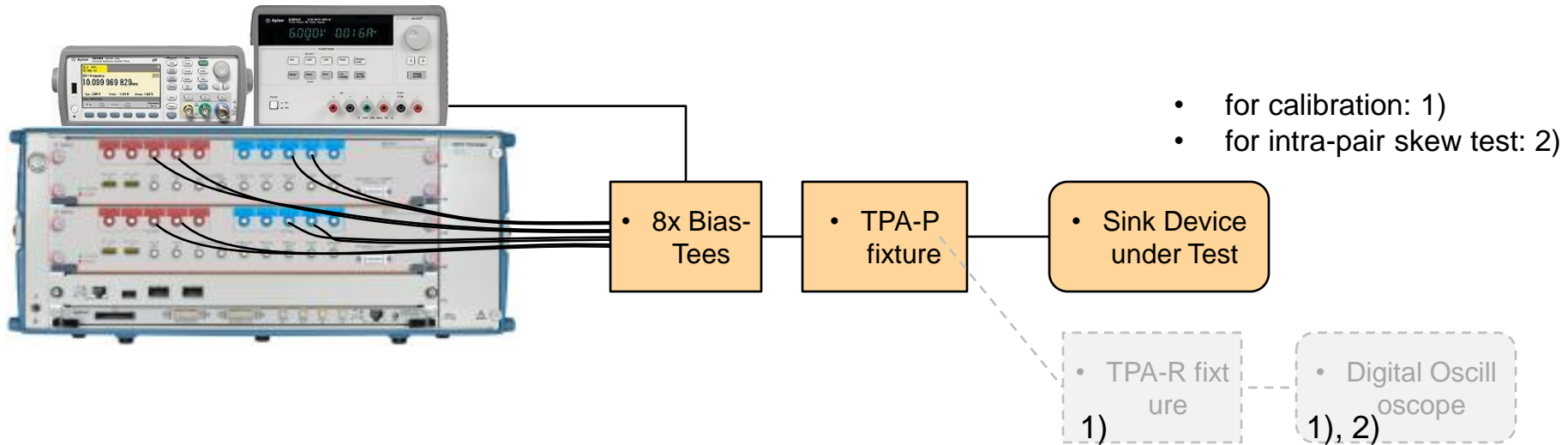


Sink

- **HF2-1** : Min/Max Differential Swing
- **HF2-2** : Intra-Pair Skew
- **HF2-3** : Jitter Tolerance
- **HF2-6** : 2160p 24-bit Color Depth
- **HF2-7** : 2160p Deep Color
- **HF2-8** : 2160p 3D
- **HF2-23** : YCBCR 4:2:0
- **HF2-24** : YCBCR 4:2:0 Deep Color
- **HF2-36** : Non-2160p 24-bit Color
- **HF2-37** : Non-2160p Deep Color
- **HF2-38** : Non-2160p 3D

Rx Test Setup with M8190A AWG

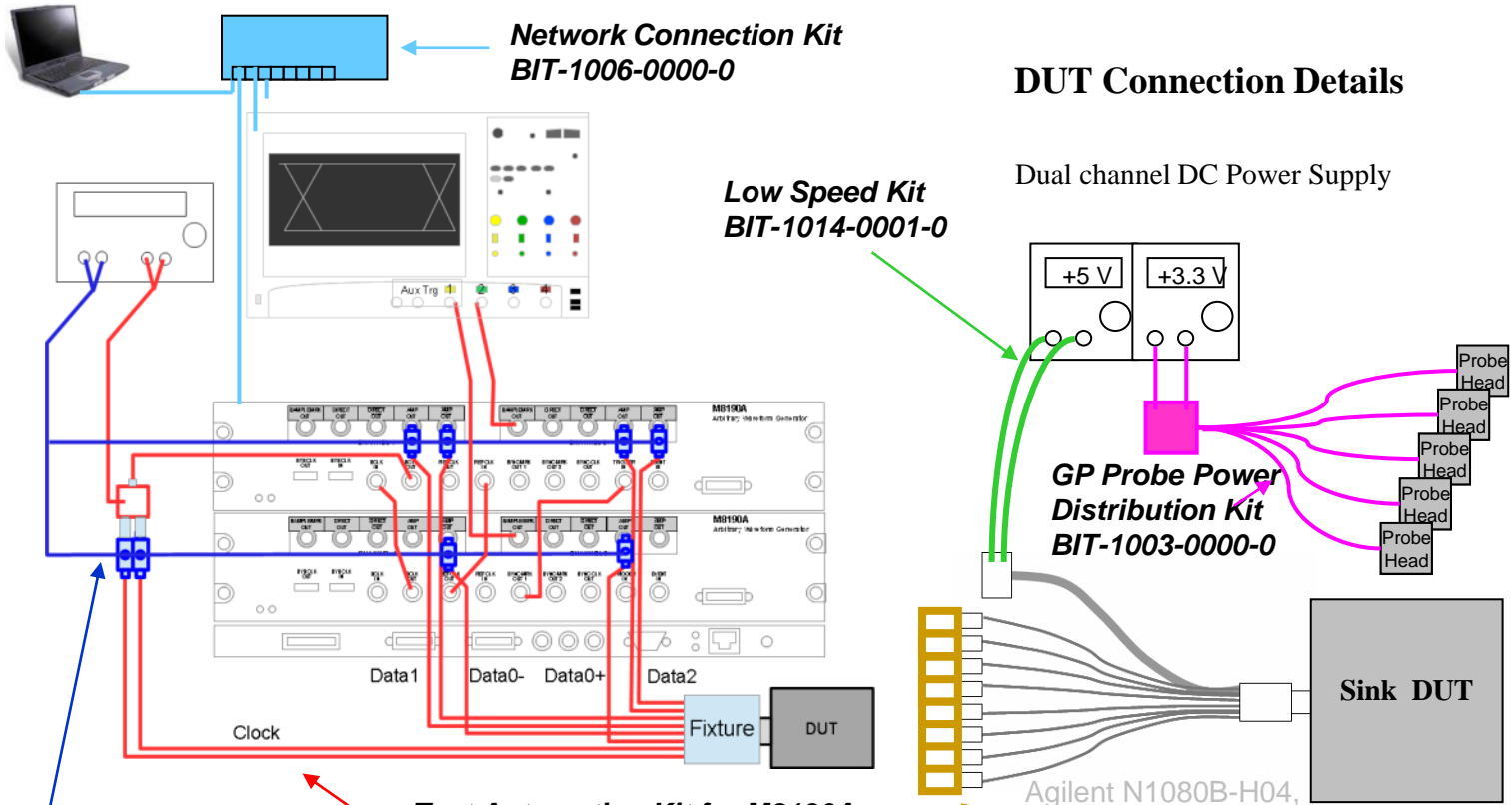
Overview



- **5-slot AXle chassis with embedded controller and two M8190A modules**
 - 4 differential channels
- **Triple output power supply and frequency counter**
- **Oscilloscope for calibration and intra pair skew test (and Tx tests)**
- **No hardware cable emulators, no TTCs**
 - Fewer manual re-connections, better reliability
- **Smaller and more affordable setup compared to ParBERT/E4887A**
 - ParBERT still better suited for characterization since jitter can be easily changed on-the-fly

HDMI 1.4b Legacy Testing

Test Accessories for M8190A AWG



Network Connection Kit
BIT-1006-0000-0

Low Speed Kit
BIT-1014-0001-0

DUT Connection Details

Dual channel DC Power Supply

GP Probe Power Distribution Kit
BIT-1003-0000-0

Sink DUT

Agilent N1080B-H04,
N1080B-H06

Snap-On Connector Kit
BIT-1005-0000-0
(40 connectors)

Bias Tee Kit for M8190A
BIT-1012-0009-0

- 8 Bias Tees
- 8 Cables SMP 0.3 m
- 1 Power Distribution (10 SMB ports)

Test Automation Kit for M8190A
BIT-1014-0009-0

- 6 Matched SMA Cable Pairs 1.0 m
- 4 SMA Cables 0.2 m
- 1 Frequency Divider incl. Power Connection Cables
- 2 BNC-to-SMA Adapters
- 1 SMA 50 Ohm Termination

N5990A Automation Software – HDMI 2.0 Rx Test Compliance Tests and Product Characterization

AWG: Opt. 151
E4887A: Opt. 150

The screenshot displays the N5990A Test Automation Software Platform interface. The main window shows a test tree on the left with 'ID HF2-2: Intra-Pair Skew Data0 2.8 Vicm' selected. The right pane shows properties for this test, including 'Sequencer' options. A 'Configure Product' dialog box is open in the foreground, showing fields for Product Number, Product Type, and Sink Test Configuration.

N5990A Automation Software – HDMI 1.4b Rx Test Compliance Tests and Product Characterization

The screenshot displays the N5990A Test Automation Software Platform interface. The main window is titled "N5990A Test Automation Software Platform" and features a menu bar (File, Station, Sequencer, Help) and a toolbar with icons for Configure DUT, Load, Save, Start, Abort, Pause, Print, Properties, and Log List. The central area is a tree view showing a test hierarchy. Under "HDMI 1.4", the test "ID 8-7: Jitter Tolerance 1920x1080p60Hz24 Jitter only on Clock" is selected and highlighted in blue. To the right, a properties window for this test is open, showing various parameters and their values. Below the tree view, a log window displays a list of messages with columns for Severity, Message, and Date.

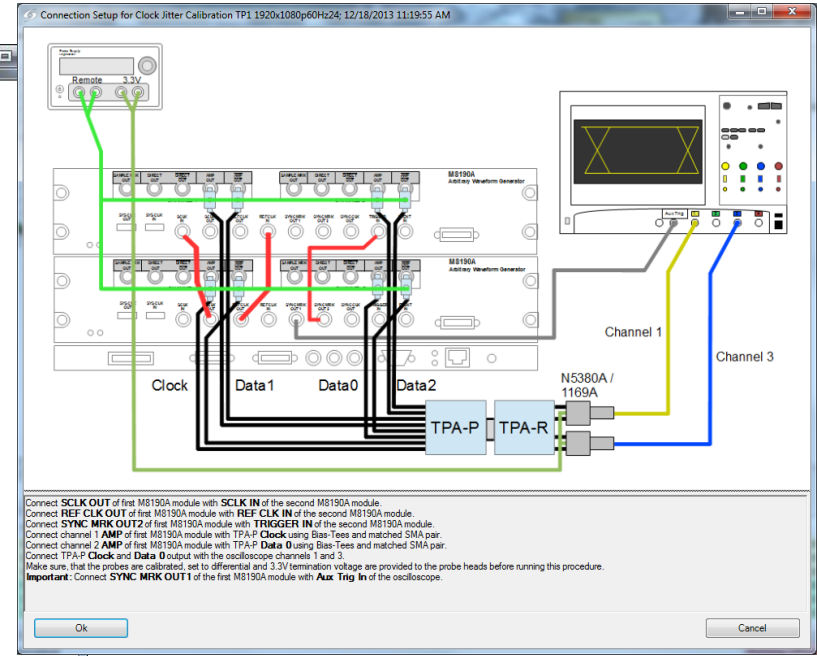
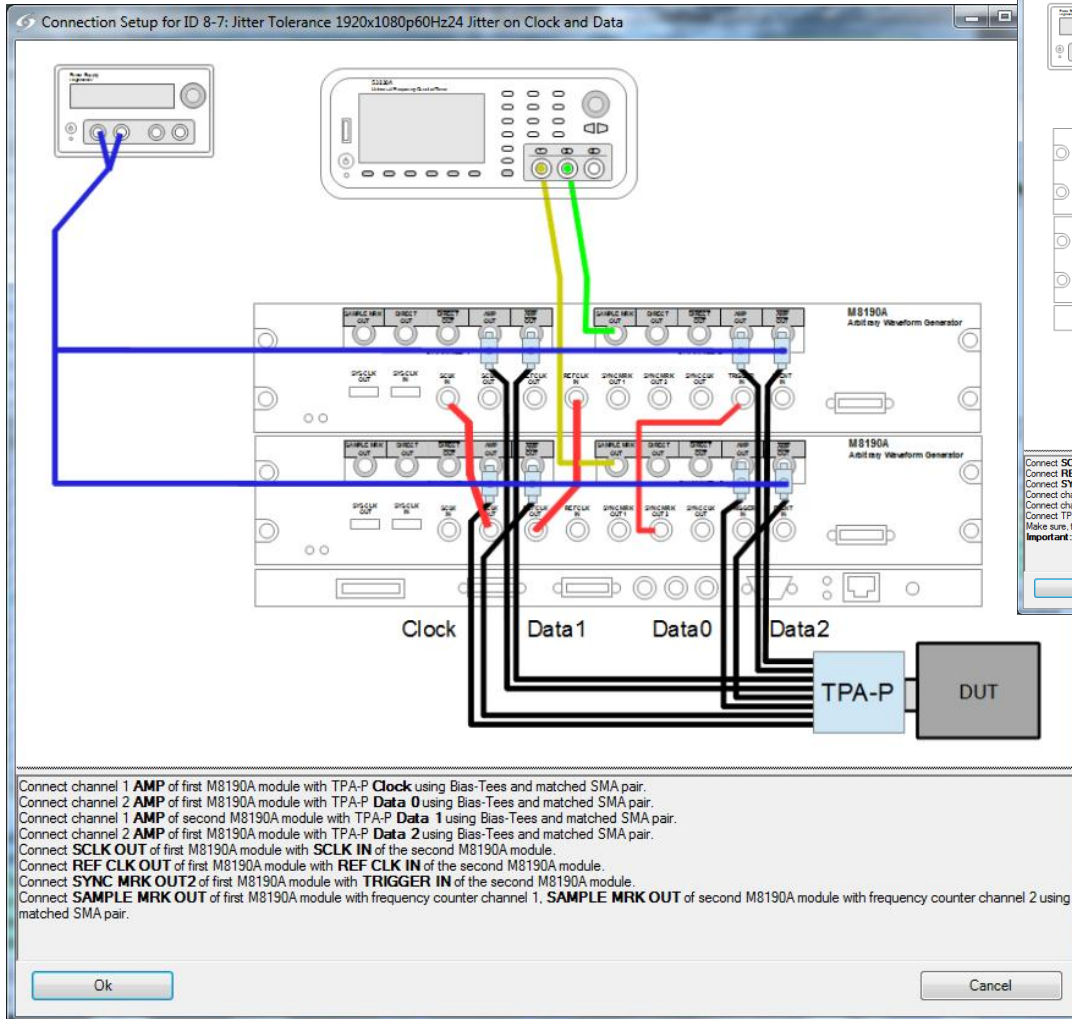
Severity	Message	Date
Progress	Opening offline connection to M8190A at TCP/IP0.:192.168.0.135:hislp6::INSTR	12/18/2013 11:14:37 AM
Progress	Opening offline connection to 53230A at TCP/IP0.:192.168.0.131:inst0::INSTR	12/18/2013 11:14:37 AM
Progress	Opening offline connection to E363xA at GPIB0.:5::INSTR	12/18/2013 11:14:37 AM
Progress	Opening offline connection to 88x_Series at 192.168.0.150	12/18/2013 11:14:37 AM
Progress	Opening offline connection to N5998A at Unknown	12/18/2013 11:14:37 AM
Info	N5990A Test Automation Software Platform startup complete!	12/18/2013 11:14:38 AM

Ready Not Running HDMI Station

legacy tests,
mandatory

HDMI 2.0 N5990A “ValiFrame” Rx Tests

Test Automation Software – Connection Diagram Examples



Calibration (with oscilloscope)

Tests (with frequency counter; 80000 or 90000 series oscilloscope required for intra pair skew test)

THANK YOU