



DATA SHEET

7411 LP5-496 Interposer

OSCILLOSCOPE PROBING SOLUTIONS

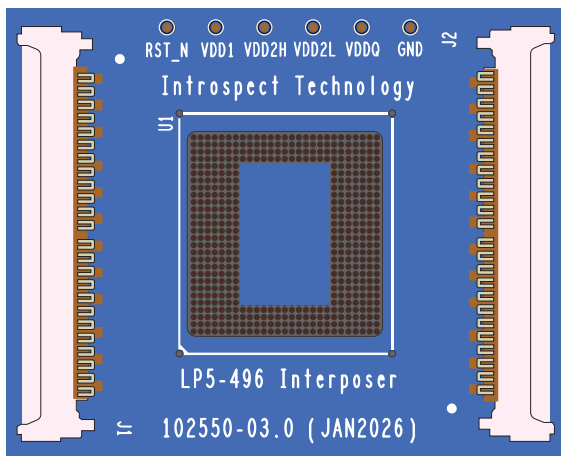


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Introduction

OVERVIEW

The 7411 LP5-496 Integrated-tip Interposer provides solderless probing access for LPDDR5 memory package-on-package (PoP) applications. It enables engineers to sense signals from beneath a memory device without requiring external soldered probe tips. By preserving the original signal path and using an integrated-tip probing interface matched to Introspect Technology's Remote Sampling Head (RSH2 or RSH3), the interposer helps minimize loading and maintain signal fidelity during measurement. Sensed signals can be connected to any 50 Ohm Oscilloscope for electrical validation or to Introspect Technology protocol analyzer products for LPDDR5 traffic capture, protocol decode, triggering, and timing analysis.



Figure 1: Typical Application

KEY FEATURES

- Supports LPDDR5 496-ball PoP Quad x16 Channel FBGA (0.4 mm pitch).
- Provides solderless Channel A signal access for CK, DQS/RDQS, DQ, CA, CS, CKE, DMI, and WCK signals.
- Integrated-tip technology tuned for RSH2 and RSH3 active probe amplifiers.
- Installs with a standard BGA rework station.
- Supports oscilloscope and protocol analyzer probing.

ORDERING INFORMATION

Table 1: When Used with RSH2

ITEM CODE	DESCRIPTION	NOTES
7411	LP5-496 Interposer with I-PEX Connectors	Main interposer part number
4884	I-PEX CA2 50P-to-Dual-30P Y-Cable	Micro-coaxial cable assembly used to connect the interposer to an adapter that is attached to the RSH2 Remote Sampling Head
6318	RSH2 I-PEX CA2 30P Adapter. Mates with 4875, 4884, 4885, and Any I-PEX 30P CA2 Cable Harness	Adapter for attachment to RSH2 Remote Sampling Head
7102	RSH2 DC - 8 GHz, 12-Channel DC-Coupled Remote Sampling Head	Active probe amplifier

Dimensions and Mechanical Drawings

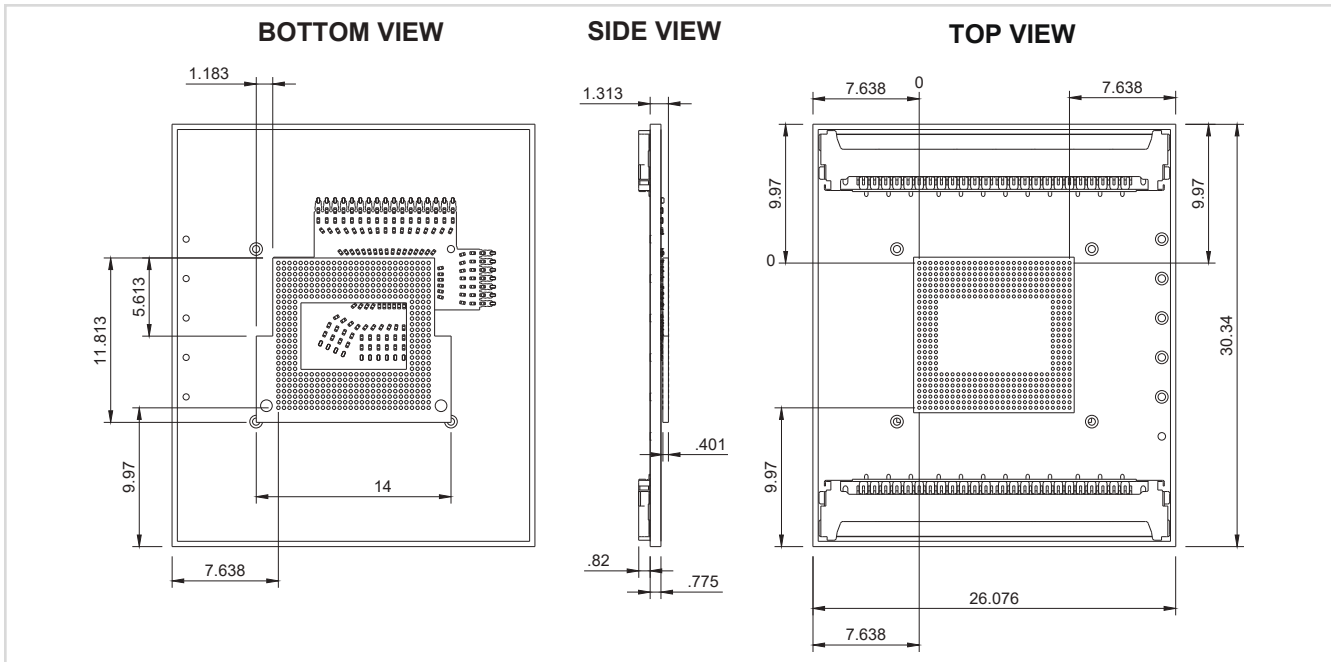


Figure 2: Mechanical Dimensions (in mm)

Signal Mappings on the Interposer

The LP5-496 Interposer **J1** and **J2** connectors route signals from the LPDDR5 memory package balls to the micro-coaxial cable assemblies. **J1** carries the command/address and control-side signals: CA[6:0], CK_T, and CS[1:0] in one cable bundle identified here as Group I. **J2** carries the data-side signals: DQ [15:0], DMI[1:0], RDQS[1:0] true/complement, and WCK[1:0] true legs and are grouped separately by two cable bundles identified here as Groups II and III.

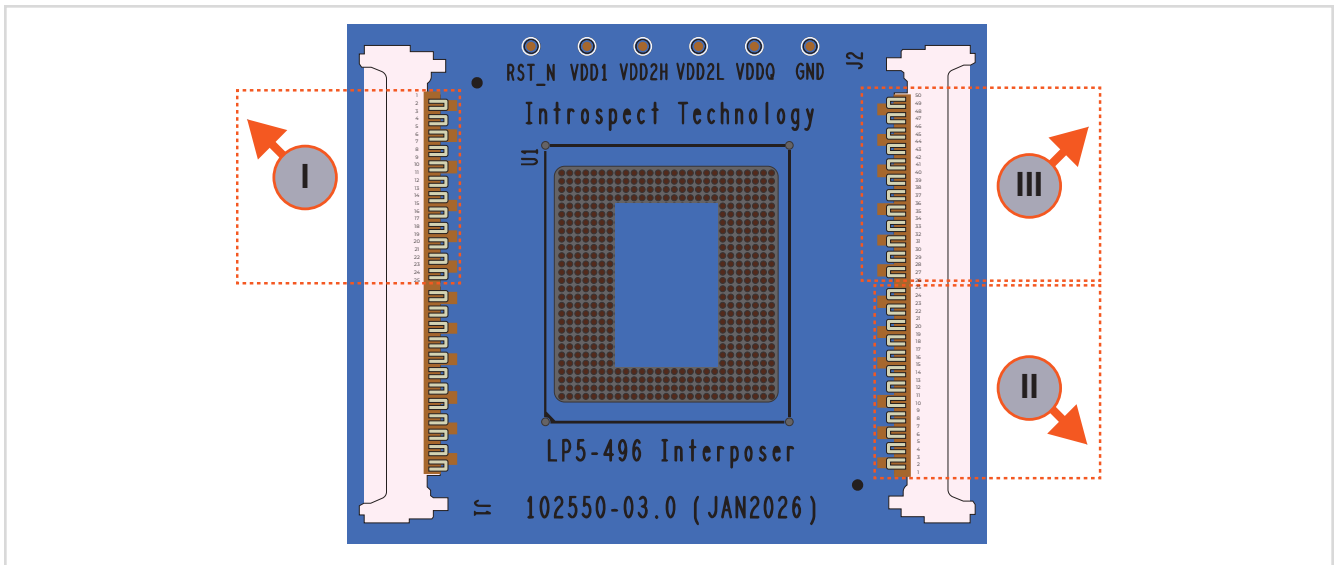


Figure 3: Pin Groupings

SIGNAL MAPPING ON J1 (GROUP I) OF THE 7411 LP5-496 INTERPOSER

PIN NUMBER	SIGNAL
1	GND
2	CA1_A
3	GND
4	CK_T_A*
5	GND
6	CA5_A
7	GND
8	CA3_A
9	GND
10	CA2_A
11	GND
12	CA0_A
13	GND
14	CS1_A
15	GND
16	CS0_A
17	GND
18	CA4_A
19	GND
20	CA6_A
21	GND
22	GND
23	NA
24	GND
25	NA

* Only the CK true-leg signal is routed in this interposer configuration. The CK complement-leg signal is not assigned in this mapping.

NA means "not assigned".

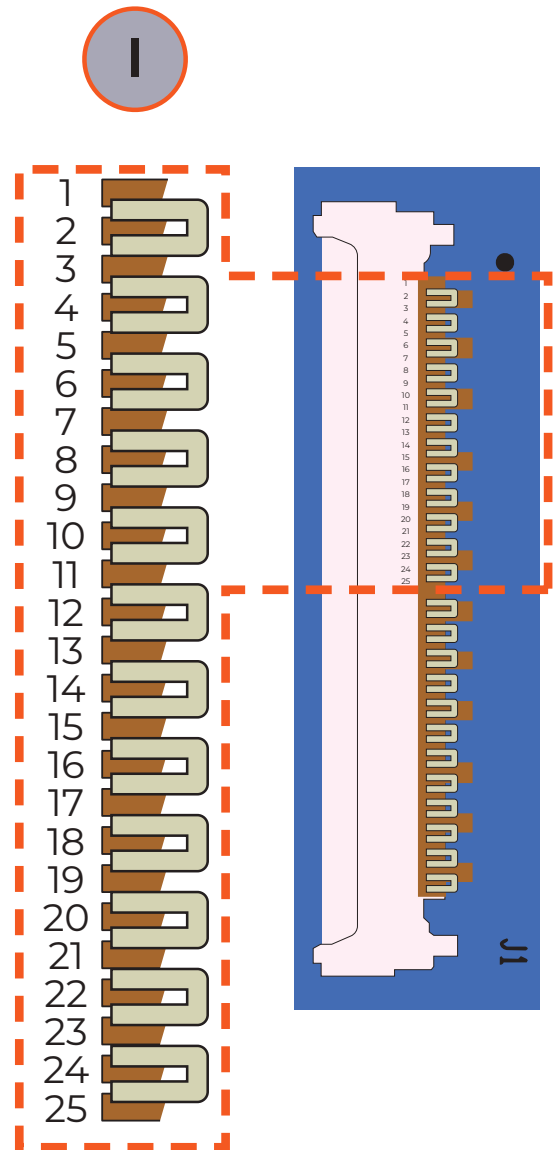
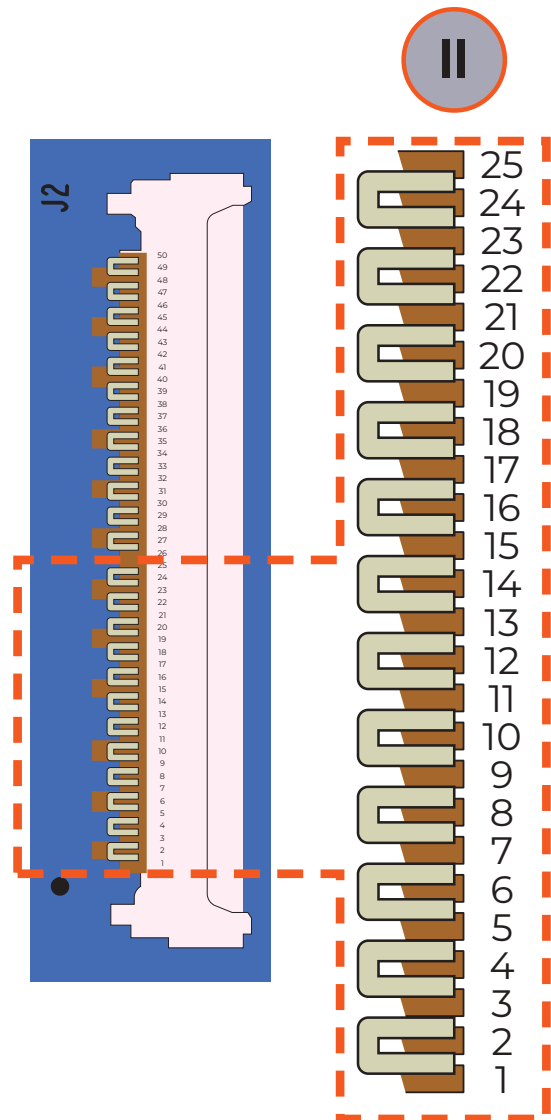


Figure 4: Interposer Pin Assignments

SIGNAL MAPPING ON J2 (GROUP II) OF THE 7411 LP5-496 INTERPOSER

PIN NUMBER	SIGNAL
25	GND
24	DQ7_A
23	GND
22	DQ5_A
21	GND
20	DQ6_A
19	GND
18	DMI0_A
17	GND
16	RDQS0_T_A
15	GND
14	RDQS0_C_A
13	GND
12	WCK0_T_A**
11	GND
10	DQ0_A
9	GND
8	DQ4_A
7	GND
6	DQ2_A
5	GND
4	DQ1_A
3	GND
2	DQ3_A
1	GND



** Only the WCK true-leg signals are routed in this interposer configuration. The WCK complement-leg signals are not assigned in this mapping.

Figure 5: Interposer Pin Assignments

SIGNAL MAPPING ON J2 (GROUP III) OF THE 7411 LP5-496 INTERPOSER

PIN NUMBER	SIGNAL
50	GND
49	DQ8_A
48	GND
47	DQ9_A
46	GND
45	DQ11_A
44	GND
43	RDQS1_C_A
42	GND
41	RDQS1_T_A
40	GND
39	DM11_A
38	GND
37	DQ14_A
36	GND
35	DQ13_A
34	GND
33	DQ10_A
32	GND
31	WCK1_T_A
30	GND
29	DQ12_A
28	GND
27	DQ15_A
26	GND

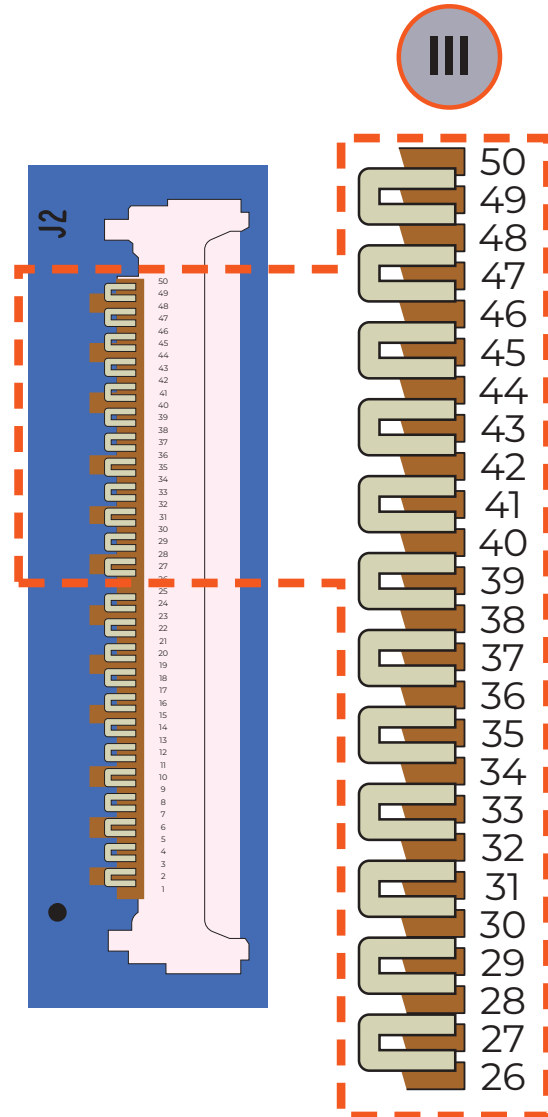


Figure 6: Interposer Pin Assignments

ADDITIONAL PROBING POINTS

The LP5-496 Interposer includes additional solder-pad probing points for sensing the LPDDR5 reset signal and memory-device power rails. These pads are provided for setup, bring-up, and debug measurements. They are separate from the high-speed signal paths routed through the I-PEX connectors and are not part of the RSH2 active-probe signal mapping.

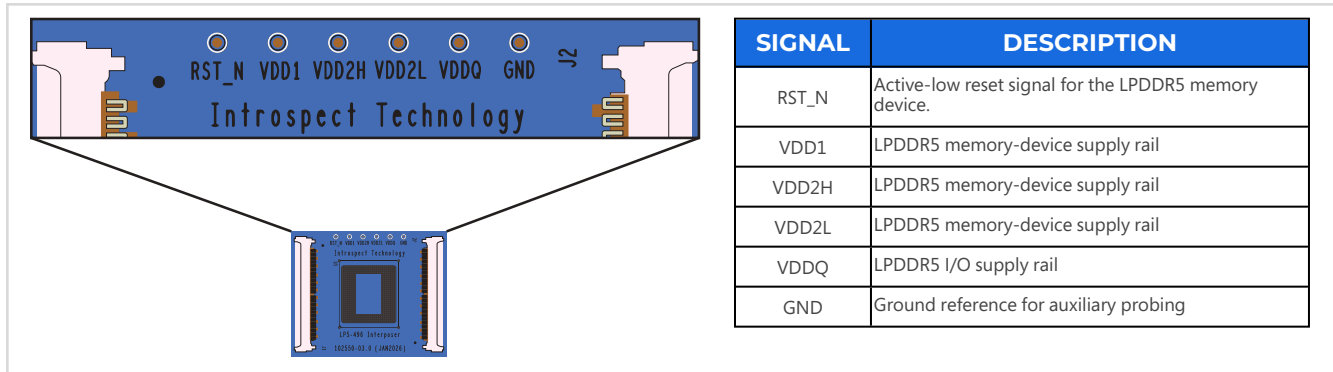


Figure 7: Additional Probing Points

NOTE

Do not connect the I-PEX connector outputs directly to an oscilloscope or to a third-party active probe. The I-PEX signal outputs are designed for connection to Introspect Technology RSH2 or RSH3 active probe amplifiers. Direct connection or third-party probing will not produce a valid signal.

Signal Mappings on RSH2

If you are using the 7411 LP5-496 Interposer with an RSH2, then this section describes the final signal routing from the memory pad locations all the way to the output of the RSH2.

Because the interposer provides access to more signals than a single RSH2 can support, you may need to connect more than one RSH2 unit to a single interposer. The system diagram below shows the complete RSH2 connection arrangement. As can be seen, a total of three distinct RSH2 units are required to access all supported signals on the interposer simultaneously.

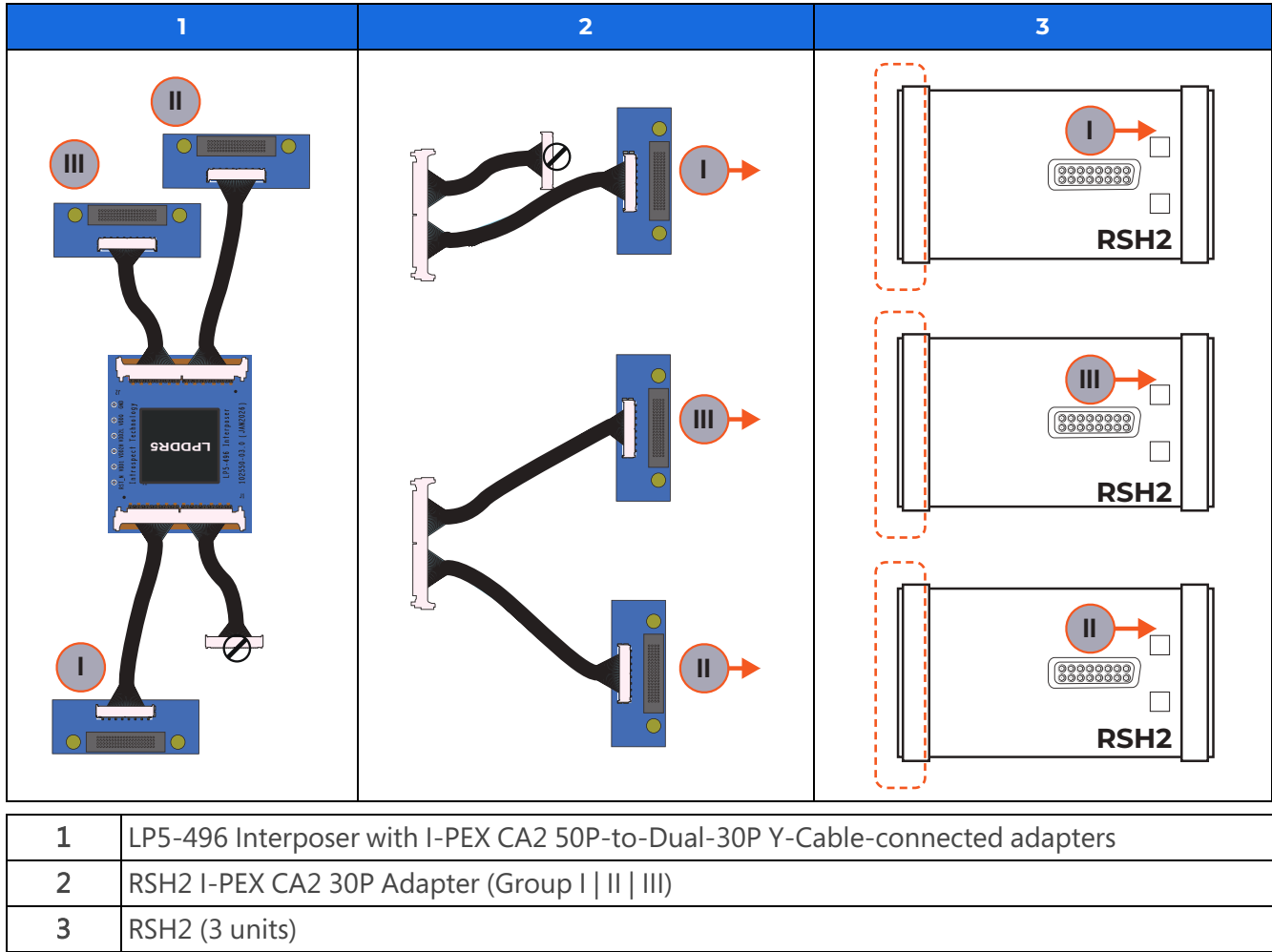
For oscilloscope probing, you may connect only one RSH2 unit at a time, depending on the signal group you want to observe. For full protocol analysis applications, all three RSH2 units are used simultaneously.

This section identifies the three RSH2 connections by signal group:

- Group I lists the signals connected to the first RSH2 unit.
- Group II lists the signals connected to the second RSH2 unit.
- Group III lists the signals connected to the third RSH2 unit.

SYSTEM DIAGRAM FOR ALL-SIGNAL ACCESS

Refer to the following system diagram for the complete solution.

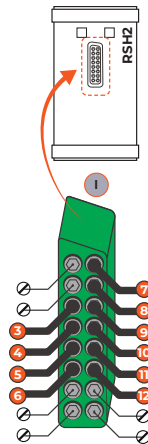


RSH2 GROUP I SIGNAL MAPPING

This table maps the LP5-496 Interposer Group I command and clock signals to the corresponding RSH2 channels.

Table 2: Group I Signal Map

MEMORY SIGNAL	RSH2 CH
NC	1
NC	2
CA6_A	3
CA4_A	4
CS0_A	5
CS1_A	6



MEMORY SIGNAL	RSH2 CH
CA1_A	7
CK_T_A	8
CA5_A	9
CA3_A	10
CA2_A	11
CA0_A	12

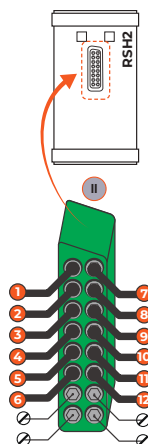
NC means "no connection".

RSH2 GROUP II SIGNAL MAPPING

This table maps the LP5-496 Interposer Group II byte-lane data, strobe, mask, and write-clock signals to the corresponding RSH2 channels.

Table 3: Group II Signal Map

MEMORY SIGNAL	RSH2 CH
DQ7_A	1
DQ5_A	2
DQ6_A	3
DMI0_A	4
RDQS0_T_A	5
RDQS0_C_A	6

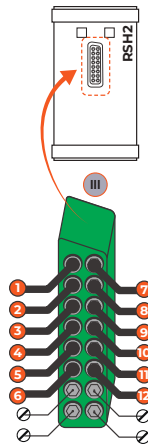


MEMORY SIGNAL	RSH2 CH
DQ3_A	7
DQ1_A	8
DQ2_A	9
DQ4_A	10
DQ0_A	11
WCK0_T_A	12

RSH2 GROUP III SIGNAL MAPPING

This table maps the LP5-496 Interposer Group III byte-lane data, strobe, mask, and write-clock signals to the corresponding RSH2 channels.

Table 4: Group III Signal Map



MEMORY SIGNAL	RSH2 CH	MEMORY SIGNAL	RSH2 CH
DQ8_A	1	DQ15_A	7
DQ9_A	2	DQ12_A	8
DQ11_A	3	WCK1_T_A	9
RDQS1_C_A	4	DQ10_A	10
RDQS1_T_A	5	DQ13_A	11
DMI1_A	6	DQ14_A	12

NOTE

For a complete end-to-end signal mapping information from the LP5-496 Interposer to the Protocol Analyzer, go to "Appendix" on page 25.

Installation Procedures

PREPARATION OF THE MEMORY DEVICE

Confirm that the memory device is a compatible BGA package supported by the LP5-496 Interposer. Do not proceed if the package ball count, package outline, or signal assignment does not match the interposer specification.

If the memory device is new and already has the specified solder ball type, it is ready for attachment to the interposer. If the solder balls are damaged, contaminated, or not the specified solder ball type, clean and re-ball the package before installation.

PARAMETER	VALUE
Memory Type	LPDDR
Memory Generation	LPDDR5
Package Type	BGA
Ball Count	496
Solder Ball Type	0.45 mm, Sn42/Bi57.6/Ag0.4, low-temperature solder balls

CAUTION

The following procedures involve BGA handling and solder reflow and must be performed only by qualified personnel using appropriate equipment. Install the LPDDR5 memory package and the interposer assembly as separate controlled steps as in "Memory Installation Procedure" on the next page and "Interposer Assembly Installation Procedure" on page 19.

Do not reflow the LPDDR5 memory package and interposer to the device under test (or DUT) at the same time unless that process has been specifically qualified. Control heating carefully and do not exceed the specified temperature limits for the interposer or DUT.

MEMORY INSTALLATION PROCEDURE

The LP5-496 Interposer is supplied as an assembled interposer board. Use the following procedure to install the LPDDR5 memory package onto the interposer before attaching the I-PEX CA2 50P-to-Dual-30P Y-Cable with adapters and connecting to the Remote Sampling Head.

1. **Remove the LPDDR5 memory package from the memory board (DUT).**

Remove the LPDDR5 memory package carefully as shown in Figure 8 below and set both the LPDDR5 memory package and DUT aside before the next step.

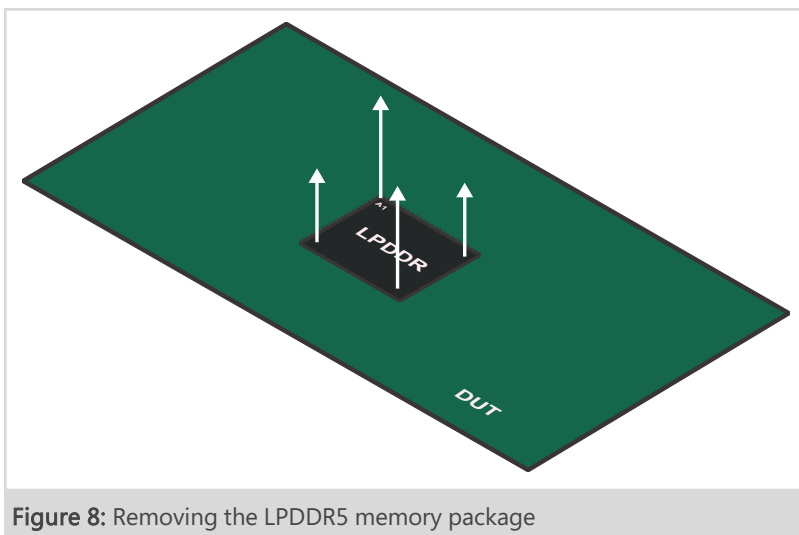


Figure 8: Removing the LPDDR5 memory package

2. **Apply flux.**

Apply flux evenly to the BGA landing area on the LP5-496 Interposer as shown in Figure 9 below.

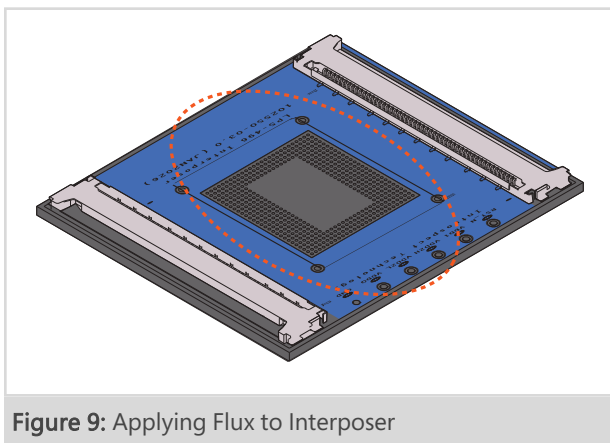


Figure 9: Applying Flux to Interposer

3. **Align the LPDDR5 memory package.**

Use a microscope or other optical aid to align the memory package with the BGA landing pattern on the LP5-496 Interposer. Align Ball A1 (shown as in the upper-left corner) of the LPDDR5 memory package with the lower-left corner of the BGA landing area on the interposer board as shown in Figure 10 below.

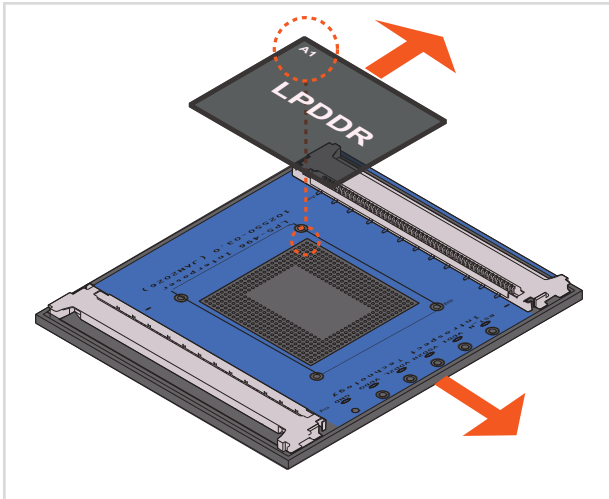


Figure 10: Aligning the Memory Module

4. **Place the LPDDR5 memory package.**

Lower the LPDDR5 memory package onto the interposer carefully into position as shown in Figure 11 below.

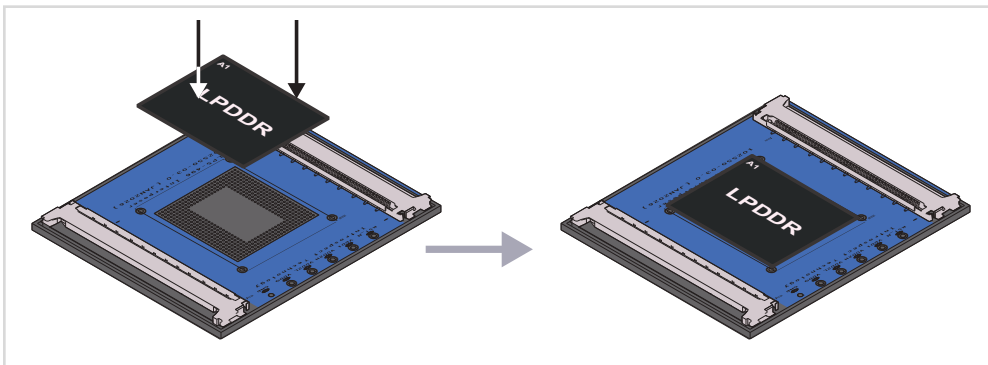


Figure 11: Installing the Memory Assembly

5. Reflow the LPDDR5 memory package assembly.

Following the temperature versus time profile as shown in Figure 12 below, reflow at no more than 204 °C (400 °F) to avoid damaging the interposer’s internal layers.

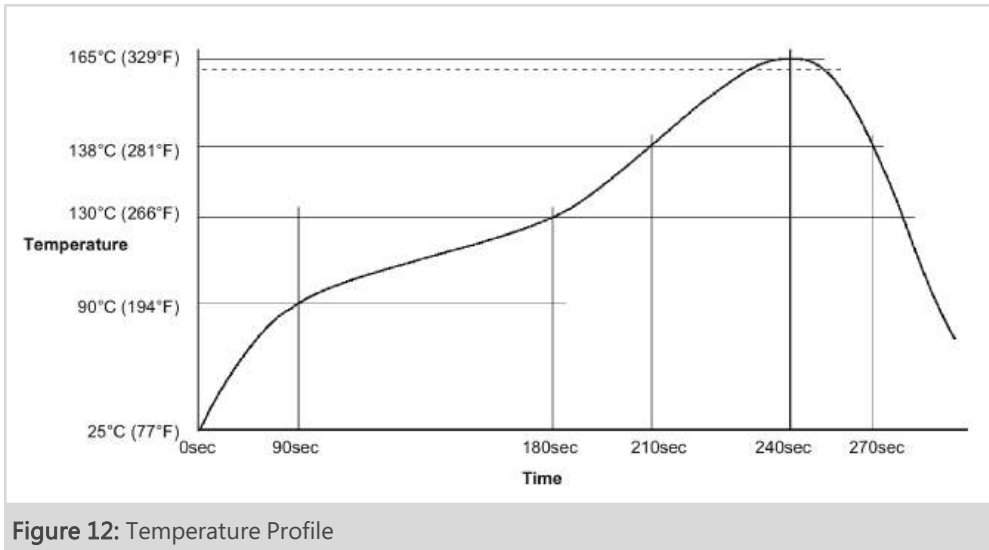


Figure 12: Temperature Profile

6. Inspect the LPDDR5 memory package assembly before the next procedure.

INTERPOSER ASSEMBLY INSTALLATION PROCEDURE

1. Clean and apply flux.

Clean the area and apply flux evenly to the BGA landing area on the DUT as shown in Figure 13 below.

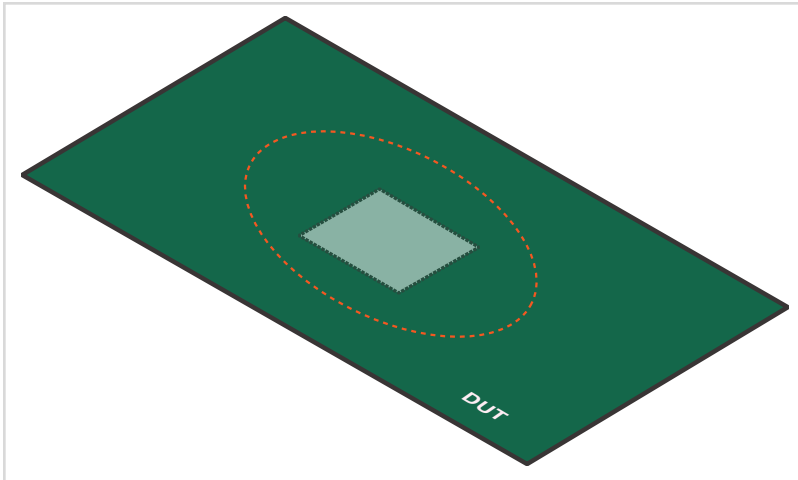


Figure 13: Applying Flux to DUT

2. Place the LPDDR5 memory package and Interposer.

Lower the LPDDR5 memory package assembly onto the DUT carefully into position as shown in Figure 14 below.

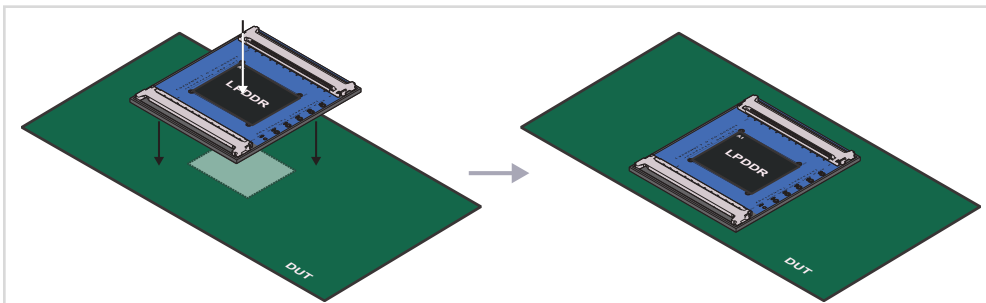


Figure 14: Installing the Interposer Assembly

3. Reflow the entire interposer assembly.

Following the temperature versus time profile as shown in Figure 12 on the previous page, reflow at no more than 204 °C (400 °F) to avoid damaging the assembly's internal layers.

4. Inspect the entire assembly after reflow.

Inspect the completed interposer assembly for proper alignment, solder bridging, insufficient wetting, and other visible defects before connecting it to the other devices in the test setup.

I-PEX CABLE AND ADAPTER ATTACHMENT PROCEDURE

Use this procedure after the completed interposer assembly has passed inspection. This procedure is intended for the end user and requires neither soldering, re-balling, nor BGA rework.

CAUTION

Do not pull on the I-PEX cables to position or disconnect the adapters. Pulling on the cables can damage the cable assembly, adapter connector, or interposer connection. Handle each adapter by the adapter body whenever possible.

1. Verify the completed interposer assembly.

Before connecting the adapters to the RSH2 units, inspect the LP5-496 Interposer assembly for proper package alignment, complete solder wetting, and absence of visible solder bridges or debris.

2. Identify the adapter groups.

Identify the adapters identified as Group I, Group II, and Group III in this guide. Each adapter corresponds to a specific signal group from the LP5-496 Interposer.

3. Attach the I-PEX CA2 50P-to-Dual-30P Y-Cable 50P-connector to the interposer connector.

In Figure 15 below left of the interposer, the I-PEX CA2 50P-to-Dual-30P Y-Cable 50P-connector is already attached to the interposer connector and the one on the right side is shown as being attached.

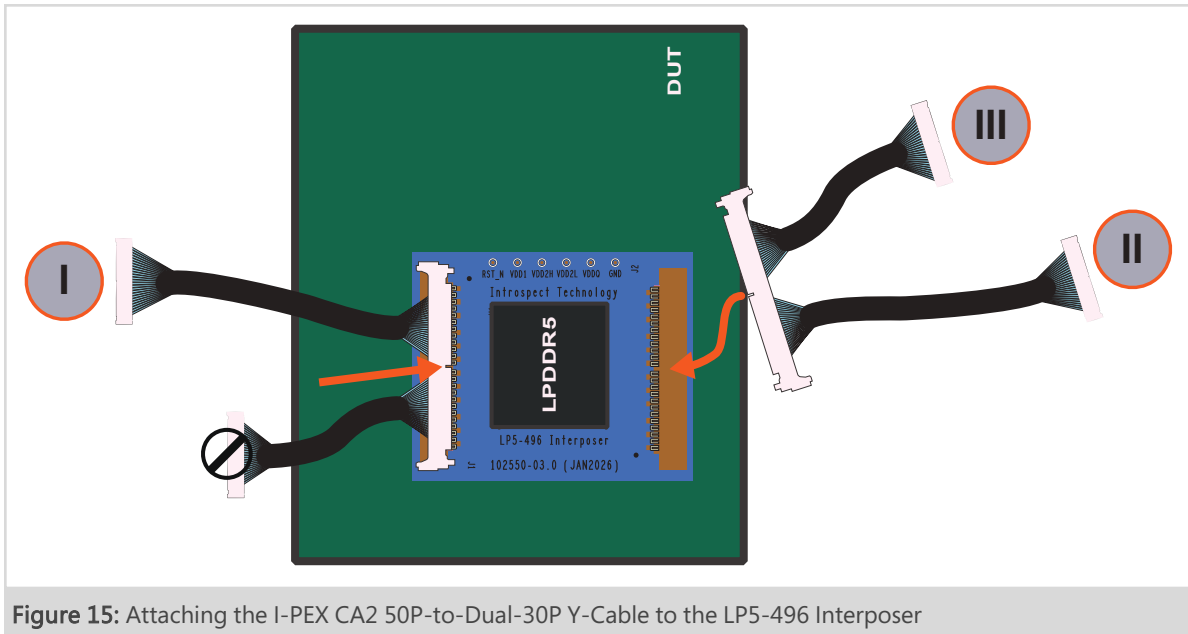


Figure 15: Attaching the I-PEX CA2 50P-to-Dual-30P Y-Cable to the LP5-496 Interposer

4. Connect each RSH2 I-PEX CA2 30P Adapter to its corresponding RSH2 unit.

Attach each assigned adapter to its corresponding RSH2 active probe amplifier. For detailed connection instructions, see the [RSH2 Remote Sampling Head Quick Start Guide](#).

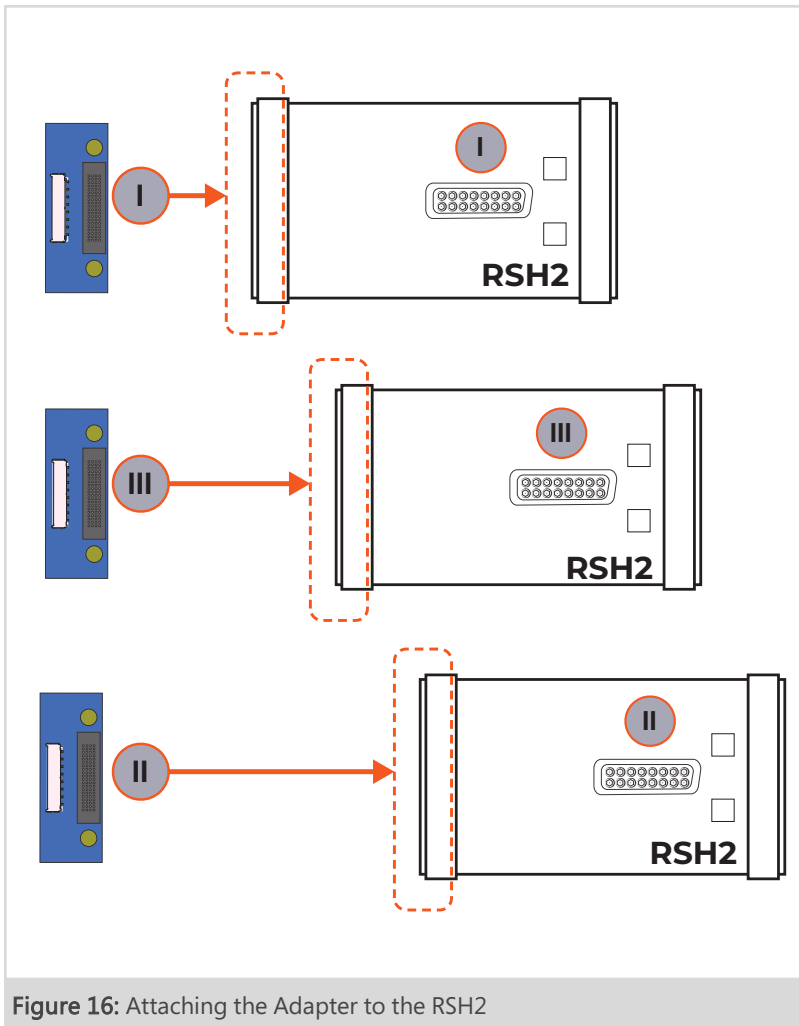


Figure 16: Attaching the Adapter to the RSH2

4. Connect each I-PEX CA2 50P-to-Dual-30P Y-Cable 30P-connector to its corresponding RSH2 I-PEX CA2 30P Adapter shown from the previous step.

Attach each assigned 30P-connector to its corresponding adapter already attached to the RSH2 active probe amplifier.

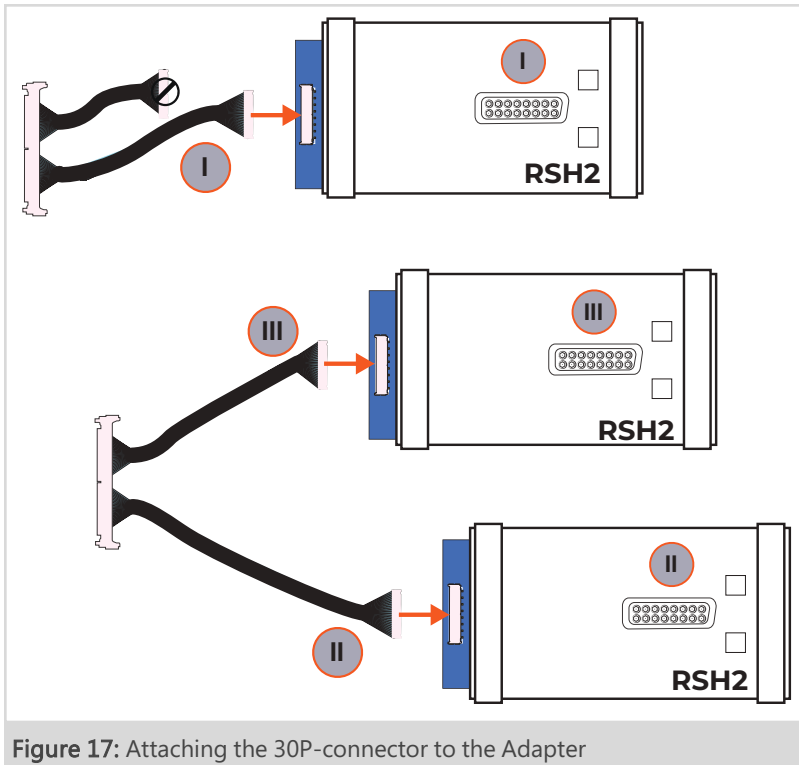


Figure 17: Attaching the 30P-connector to the Adapter

4. Verify the connections.

Confirm that each adapter is fully seated and connected to the correct RSH2 unit. Check that the cables are not pinched, sharply bent, twisted, or under tension.

5. Continue to the applicable Protocol Analyzer or 50 Ohm Oscilloscope setup.

After the adapters are connected to the RSH2 units, refer to "Appendix" on page 25 for downstream instrument configuration.

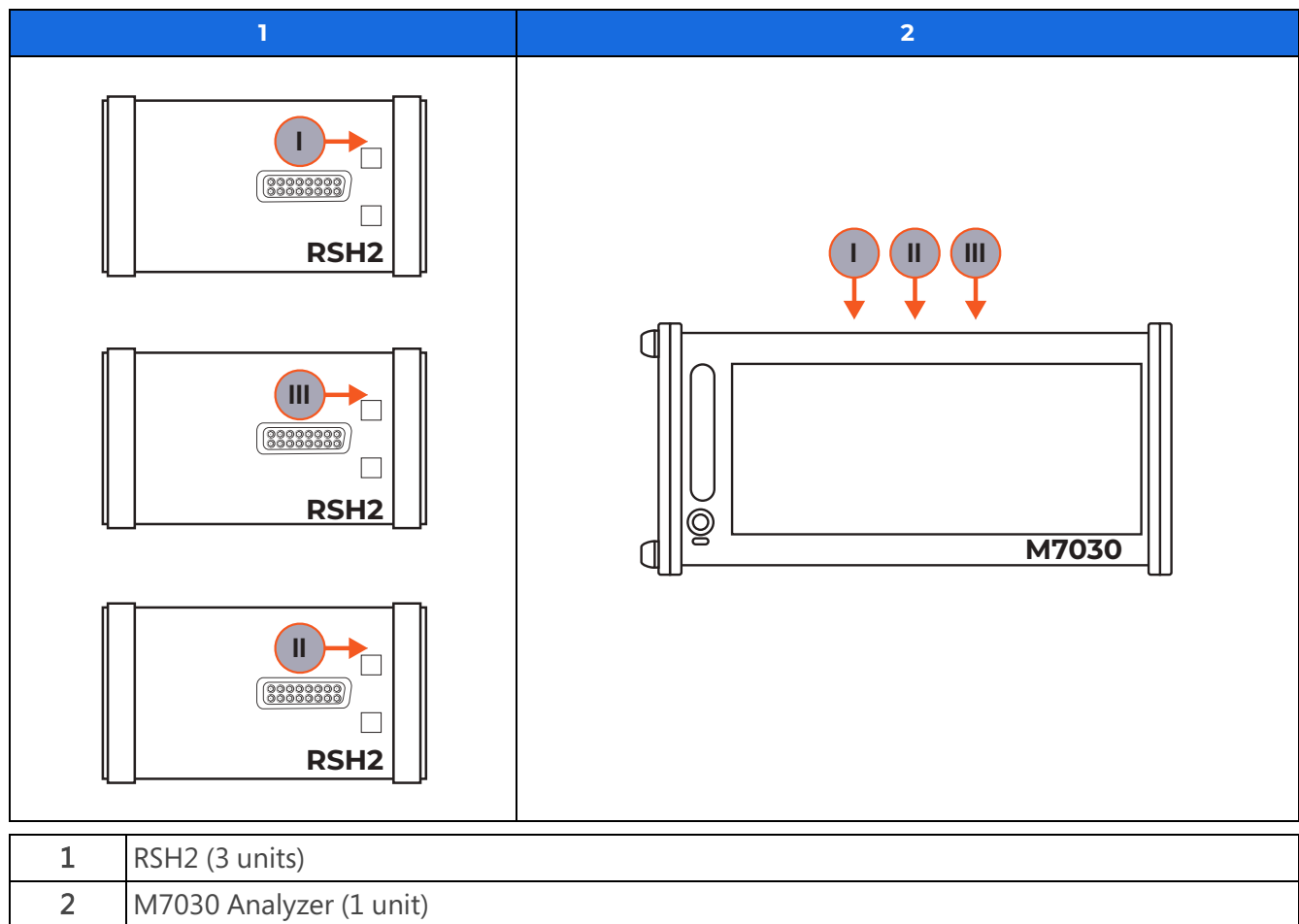
NOTE

Do not connect the I-PEX connector outputs directly to an oscilloscope or to a third-party active probe. The I-PEX signal outputs are designed for connection to Introspect Technology RSH2 active probe amplifiers. Direct connection or third-party probing will not produce a valid signal.

Appendix

M7030 ANALYZER (36 CHANNELS) THROUGH RSH2 CONNECTIONS

This section provides the signal and end-to-end channel mapping for the LP5-496 Interposer-to-RSH2-to-M7030 Analyzer configuration. Use these tables to trace each memory signal from the memory package, to the interposer and its adapters, through the Remote Sampling Head connection, to the corresponding Protocol Analyzer channel.



RSH2 to M7030 Analyzer (Group I)

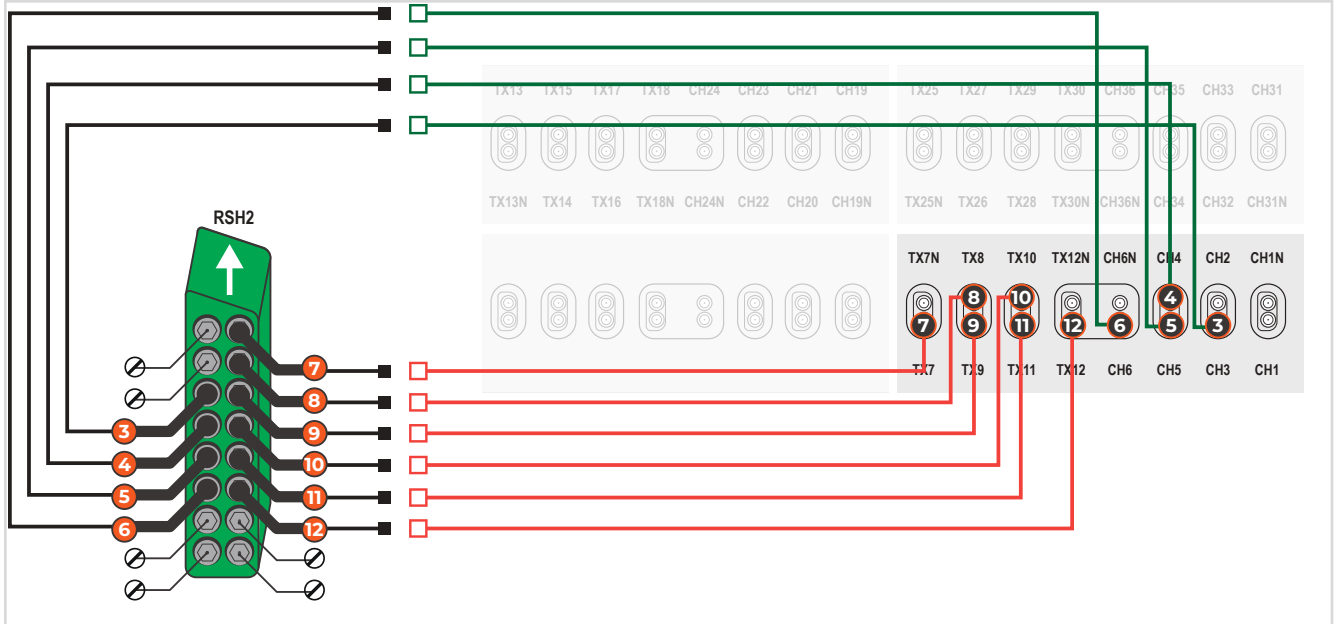


Figure 18: Wire Connections for RSH2 I-PEX CA2 30P Adapter (Group I)

Table 5: Group I End-to-End Signal Mapping

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
NC	NC	NC
NC	NC	NC
CA6_A	3	3
CA4_A	4	4
CS0_A	5	5
CS1_A	6	6

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
CA1_A	7	7
CK_T_A	8	8
CA5_A	9	9
CA3_A	10	10
CA2_A	11	11
CA0_A	12	12

NC means "no connection".

RSH2 to M7030 Analyzer (Group II)

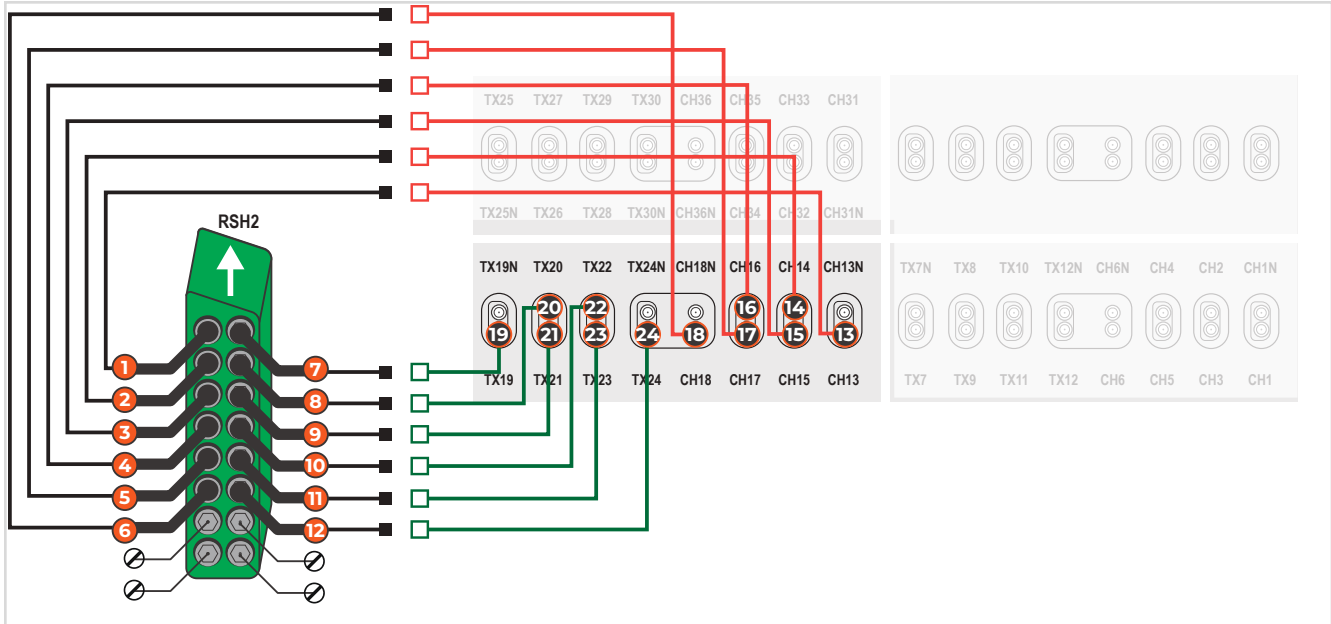


Figure 19: Wire Connections for RSH2 I-PEX CA2 30P Adapter (Group II)

Table 6: Group II End-to-End Signal Mapping

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
DQ7_A	1	13
DQ5_A	2	14
DQ6_A	3	15
DMI0_A	4	16
RDQS0_T_A	5	17
RDQS0_C_A	6	18

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
DQ3_A	7	19
DQ1_A	8	20
DQ2_A	9	21
DQ4_A	10	22
DQ0_A	11	23
WCK0_T_A	12	24

RSH2 to M7030 Analyzer (Group III)

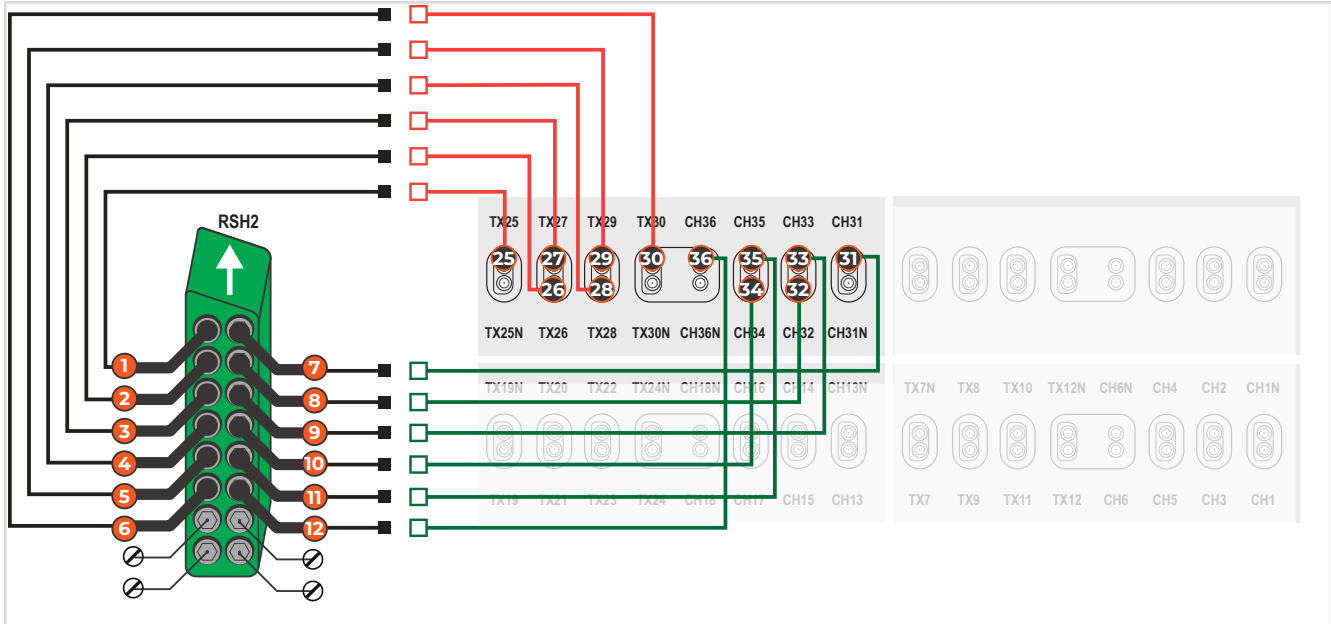


Figure 20: Wire Connections for RSH2 I-PEX CA2 30P Adapter (Group III)

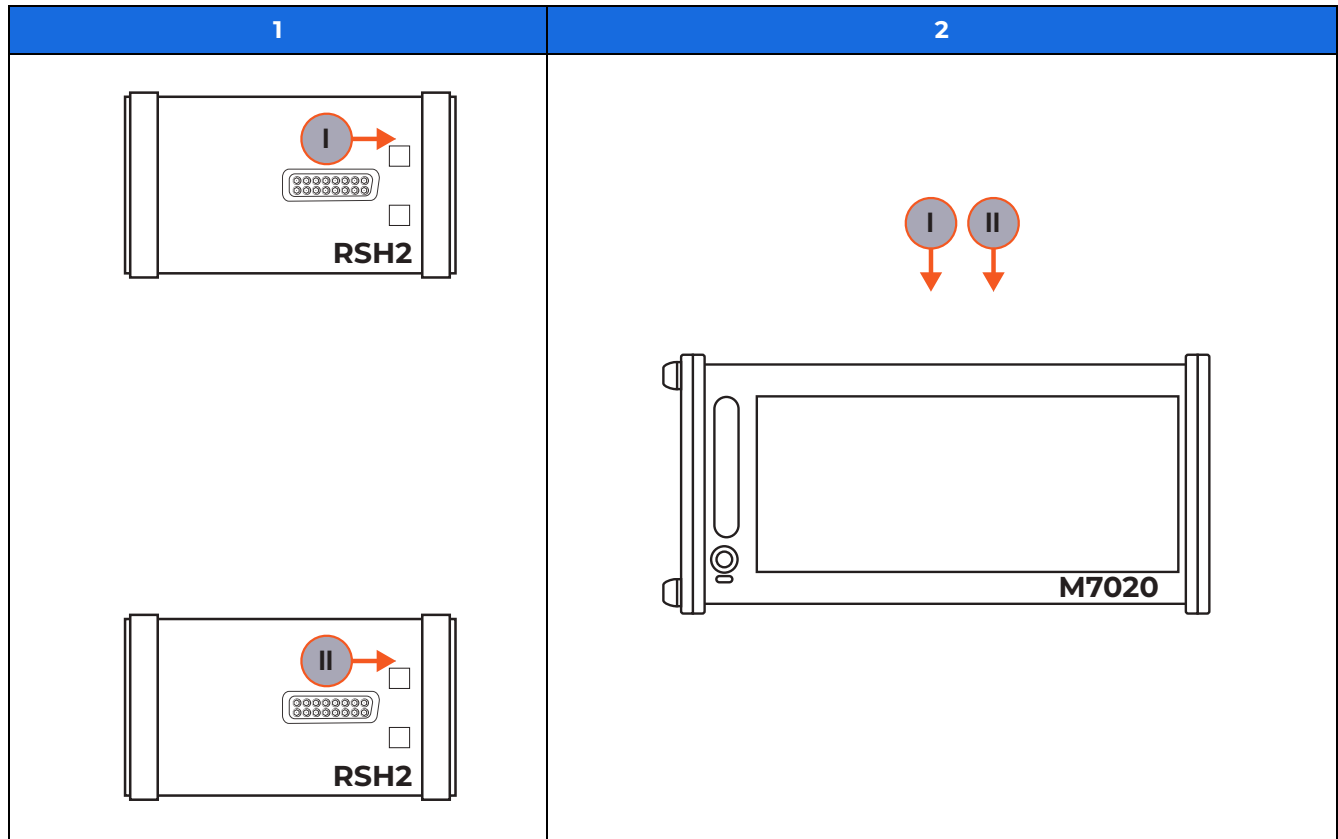
Table 7: Group III End-to-End Signal Mapping

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
DQ8_A	1	25
DQ9_A	2	26
DQ11_A	3	27
RDQS1_C_A	4	28
RDQS1_T_A	5	29
DMI1_A	6	30

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
DQ15_A	7	31
DQ12_A	8	32
WCK1_T_A	9	33
DQ10_A	10	34
DQ13_A	11	35
DQ14_A	12	36

M7020 ANALYZER (24 CHANNELS) THROUGH RSH2 CONNECTIONS

This section provides the signal and end-to-end channel mapping for the LP5-496 Interposer-to-RSH2-to-M7020 Analyzer configuration. Use these tables to trace each memory signal from the memory package, to the interposer and its adapters, through the Remote Sampling Head connection, to the corresponding Protocol Analyzer channel.



1	RSH2 (2 units)
2	M7020 Analyzer (1 unit)

RSH2 to M7020 Analyzer (Group I)

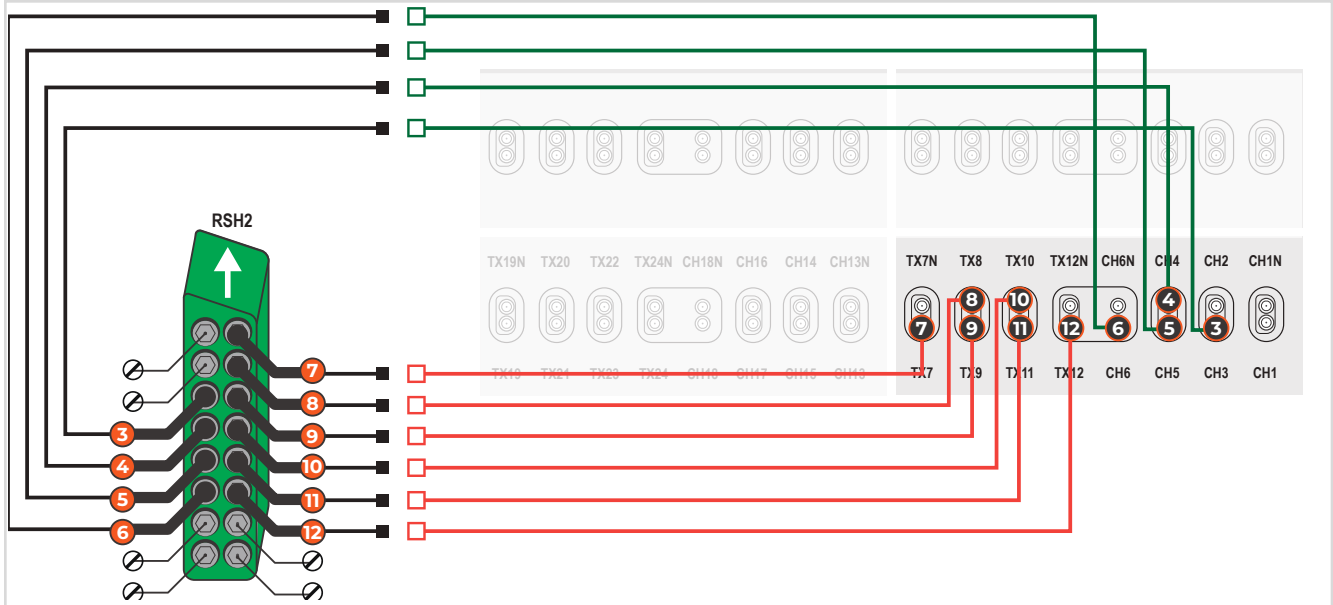


Figure 21: Wire Connections for RSH2 I-PEX CA2 30P Adapter (Group I)

Table 8: Group I End-to-End Signal Mapping

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
NC	NC	NC
NC	NC	NC
CA6_A	3	3
CA4_A	4	4
CS0_A	5	5
CS1_A	6	6

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
CA1_A	7	7
CK_T_A	8	8
CA5_A	9	9
CA3_A	10	10
CA2_A	11	11
CA0_A	12	12

NC means "no connection".

RSH2 to M7020 Analyzer (Group II)

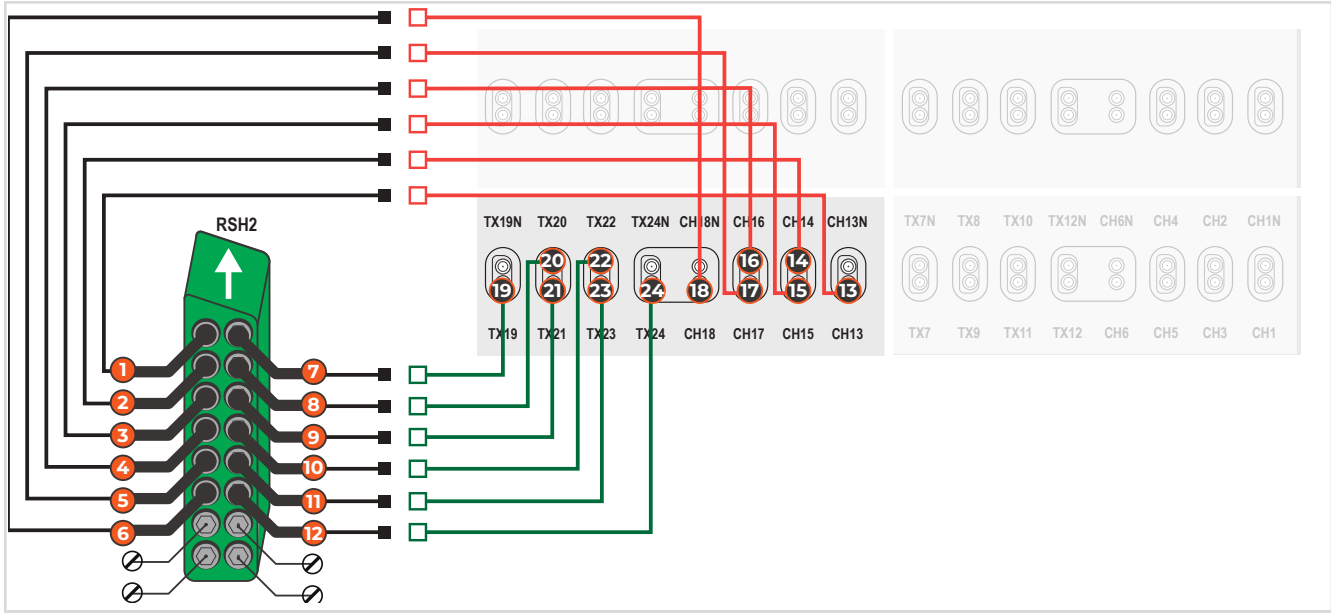


Figure 22: Wire Connections for RSH2 I-PEX CA2 30P Adapter (Group II)

Table 9: Group II End-to-End Signal Mapping

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
DQ7_A	1	13
DQ5_A	2	14
DQ6_A	3	15
DMI0_A	4	16
RDQS0_T_A	5	17
RDQS0_C_A	6	18

MEMORY SIGNAL	RSH2 CH	ANALYZER CH
DQ3_A	7	19
DQ1_A	8	20
DQ2_A	9	21
DQ4_A	10	22
DQ0_A	11	23
WCK0_T_A	12	24



REVISION NUMBER	HISTORY	DATE
1.0	Document Release.	May 21, 2026

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