



DATA SHEET

SV5C-DPTXCPTX

MIPI D-PHY / C-PHY Generator

C SERIES



Table of Contents

Introduction.....	3
Overview	3
Key Benefits	3
Applications	3
Physical Connections.....	4
MXP High Speed Connector Pinout.....	4
GPIO Connector Pinout.....	5
Power Connector Pinout.....	6
Ordering Information.....	6
Specifications	7

Introduction

OVERVIEW

The SV5C-DPTXCPTX MIPI D-PHY/C-PHY Generator is an ultra-portable, high-performance instrument that enables characterization and validation of MIPI D-PHY and C-PHY receiver ports. The instrument operates over a continuous range of data rates and includes analog parameter controls that enable deep insights into receiver voltage sensitivity, receiver skew and jitter tolerance for receiver stress-testing.

The instrument operates with the easy-to-use, highly versatile Pinetree software environment for automated physical layer compliance testing. Pinetree also includes pattern synthesis tools that enable the generation of complete DSI-2 or CSI-2 packets such as color bars and active image frames for system-level test.

This document describes the electrical characteristics and key specifications of the D-PHY and C-PHY Generator. Please refer to User Manual documentation for operating instructions.

KEY BENEFITS

- Any-rate operation to 12.5 Gbps per lane (D-PHY) and 8 Gbps per trio (C-PHY)
- Per-lane HS voltage level and common-mode control
- Per-lane LP voltage level control
- Per-lane skew injection with < 1 ps resolution
- Per-lane multi-source jitter injection
- State-of-the-art programming environment based on the highly intuitive Python language

APPLICATIONS

- Parallel physical layer validation
- DSI and CSI packet and protocol testing
- Plug-and-play system-level validation

PHYSICAL CONNECTIONS

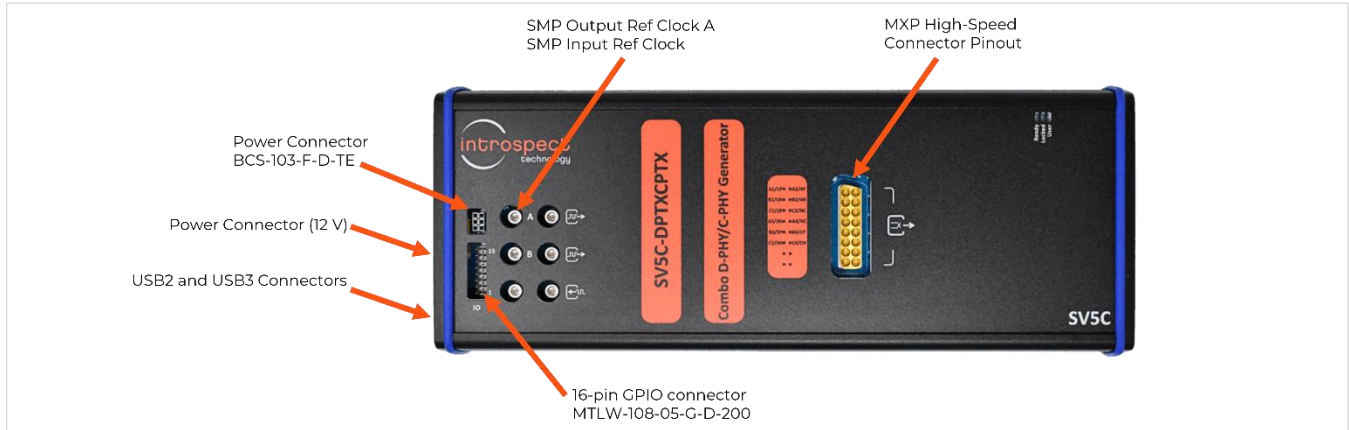


Figure 1: SV5C-DPTXCPTX physical connections.

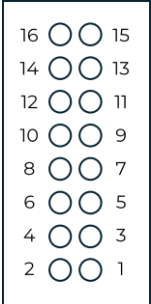
MXP HIGH SPEED CONNECTOR PINOUT

TABLE 1: SIGNAL MAPPING OF THE MXP CONNECTOR FOR SV5C-DPTXCPTX

	MXP PIN	D-PHY PINOUT	C-PHY PINOUT
<p>MXP Top View</p>	1	Data Lane 1 P	Trio 1 A
	2	Data Lane 1 N	Trio 1 B
	3	Data Lane 2 P	Trio 1 C
	4	Data Lane 2 N	Trio 3 A
	5	Data Lane 3 P	Trio 3 B
	6	Data Lane 3 N	Trio 3 C
	7	NC	NC
	8	NC	NC
	9	Data Lane 4 P	Trio 2 A
	10	Data Lane 4 N	Trio 2 B
	11	NC	Trio 2 C
	12	NC	Trio 4 A
	13	Clock Lane P	Trio 4 B
	14	Clock Lane N	Trio 4 C
	15	NC	NC
	16	NC	NC

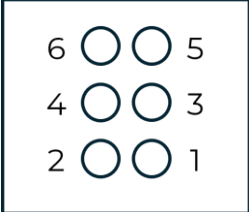
GPIO CONNECTOR PINOUT

TABLE 2: PINOUT FOR GPIO CONNECTORS

	PIN NUMBER	I/O	FUNCTION	DESCRIPTION
GPIO Connector Top View 	1	Input/Output		NC
	2	Input/Output	userio[0] / daisy_trig_out	User configurable 1.8V IO
	3	Input/Output		NC
	4	Input/Output	userio[1] / daisy_ready_out	User configurable 1.8V IO Used for aligning two SV5C-DPTXCPTX together
	5			Ground
	6	Input/Output	userio[2] / daisy_ready_in	User configurable 1.8V IO Used for aligning two SV5C-DPTXCPTX together
	7			NC
	8	Input/Output	userio[3] / Fast-BTA rqst*	User configurable 1.8V IO *Advanced high-speed bus turnaround trigger
	9			Ground
	10	Input	fw_rst_pin_n	Active low firmware reset. Minimum pulse width = 50 ns
	11			NC
	12	Input/Output	user_i2c_scl	User I2C SCL
	13	Input/Output		NC
	14	Input/Output	user_i2c_sda	User I2C SDA
	15	Output	PwrSeqAlert	Power sequencer alert
	16	Output	te_trig	Tearing effect output, rising edge triggered

POWER CONNECTOR PINOUT

TABLE 3: PINOUT FOR GPIO CONNECTORS

	PIN NUMBER	PIN NAME
 <p>Power Connector Top View</p>	1	Ground
	2	3.3V
	3	Ground
	4	1.8V
	5	Ground
	6	1.2V

ORDERING INFORMATION

TABLE 4: ITEM NUMBERS FOR THE SV5C-DPTXCPTX AND RELATED PRODUCTS

PART NUMBER	NAME	KEY DIFFERENTIATORS
5782	SV5C-DPTX	D-PHY only
5783	SV5C-CPTX	C-PHY only
5786	SV5C-DPTXCPTX	Supports both D-PHY and C-PHY
5791	Speed Upgrade 8 to 12.5 Gbps	D-PHY
5792	Speed Upgrade from 6.5 to 8 Gbps	C-PHY
5793	SV5C TX PHY Upgrade	License to add the C-PHY functionality

Specifications

TABLE 5: GENERAL SPECIFICATIONS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol Support			
Physical layer interface	D-PHY C-PHY		
MIPI protocol	CSI/DSI		Flexible pattern architecture allows for the generation of encoded PHY data, unencoded PHY data, or entire CSI/DSI frames
LP/HS Handling	Automatic		Automatically generates LP and HS data
Ports			
Number of D-PHY Lanes	4 Lanes and CLK		
Number of C-PHY Trios	4 Trios		
Number of Dedicated Output Reference Clocks	2		Individually synthesized frequency and output format
Number of Dedicated Input Reference Clocks	1		Used as external reference clock input
Number of Trigger Inputs	2		Via Molex connector
Number of Flag Outputs	2		Via Molex connector
Number of I2C/I3C Masters	1		Via Molex connector
Connections to PC for accessing Pinetree	2		USB2 and USB3
Power and Environmental Conditions			
DC Input Voltage	12	Volt	
Maximum Current Draw	6.5	Amp	12.5 Gbps / 4 Lane D-PHY operation

Maximum Current Draw	6.0	Amp	8 Gsps / 4 Trio C-PHY operation PRBS9 pattern, HS amplitude = 200 mV
Minimum Ambient Temperature	5	° C	
Maximum Ambient Temperature	35	° C	

TABLE 6: DATA RATES AND REFERENCE CLOCKS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Data Rates and Frequencies			
Minimum Programmable Data Rate	80	Mbps	D-PHY
	80	Msps	C-PHY
Maximum Programmable Data Rate	8.5	Gbps	D-PHY
	6	Gsps	C-PHY
Maximum Data Rate Purchase Options	6	Gsps	C-PHY
	8.5		
Maximum Data Rate Purchase Options	8	Gbps	D-PHY
	12.5		
Frequency Resolution of Programmed Data Rate	1	kHz	
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Supported External Input Clock I/O Standards			LVDS (typical 400 mVpp input) LVPECL (typical 800 mVpp input)
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	250	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Output Clock I/O Standards			LVDS, LVPECL, CML, HCSL, and LVCMOS

TABLE 7: HS VOLTAGE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Output Coupling			
Output Differential Impedance	100	Ohm	
Differential Impedance Tolerance	+/- 10	Ohm	
Output Single-Ended Impedance	50	Ohm	
Single-Ended Impedance Tolerance	+/- 5	Ohm	
HS Voltage Performance			
Minimum Output Voltage Amplitude	20	mV	D-PHY, differential
	20	mV	C-PHY, single ended
Maximum Output Voltage Amplitude	400	mV	D-PHY, differential
	400	mV	C-PHY, single ended
Voltage Swing Resolution	20	mV	D-PHY, differential
	20	mV	C-PHY, single ended
Voltage Swing Accuracy	>5% or 10 mV	%, mV	
Minimum Common Mode Voltage	-100	mV	D-PHY
	-400	mV	C-PHY
Maximum Common Mode Voltage	500	mV	D-PHY (can override up to 1000 mV)
	500		C-PHY (can override up to 1000 mV)
Common Mode Voltage Resolution	1	mV	D-PHY or C-PHY
Common Mode Voltage Accuracy	>5% or 10 mV	%, mV	
Rise and Fall Time	50	ps	Typical, 20% to 80%
Swing and Common Mode Setting	Per Lane		D-PHY
	Per Trio		C-PHY

TABLE 8: LP VOLTAGE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
LP Voltage Controls			
Minimum Programmable LP Logic High Level	0	mV	LP voltage control specifications apply to both D-PHY and C-PHY
Maximum Programmable LP Logic High Level	1200	mV	
Minimum Programmable LP Logic Low Level	-100	mV	
Maximum Programmable LP Logic Low Level	1000	mV	
Logic Level Control Resolution	1	mV	
Logic Level Accuracy	>5% or 10 mV	%, mV	

TABLE 9: HS JITTER AND NOISE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Jitter and Noise Performance			
Random Jitter (RMS)	< 1.3	ps rms	D-PHY, differential
Random Jitter (RMS)	< 1.7 < 1.3	ps rms ps rms	C-PHY, single ended 1.0 Gsps, HS-only 444 pattern 6.5 Gsps, HS-only 444 pattern
Minimum Frequency of Injected Deterministic Jitter	0.1	kHz	D-PHY or C-PHY
Maximum Frequency of Injected Deterministic Jitter	50	MHz	D-PHY or C-PHY
Frequency Resolution of Injected Deterministic Jitter	0.1	kHz	D-PHY or C-PHY
Maximum Peak to Peak Deterministic Jitter	2	UI	D-PHY or C-PHY , numerically generated, tested to 1000 ps
Magnitude Resolution of Injected Deterministic Jitter	500	fs	D-PHY or C-PHY
Accuracy of Injected Deterministic Jitter	>10% or 10 ps	%, ps	D-PHY or C-PHY
Common Mode Noise Injection Minimum Sinusoidal Frequency	1.044	MHz	
Common Mode Noise Injection Maximum Sinusoidal Frequency	1.3	GHz	
Common Mode Noise Injection Maximum Sinusoidal Amplitude	235	mV	Measured single ended

TABLE 10: HS CHANNEL SKEW CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Channel Skew Performance			
Coarse Skew Range: Minimum Programmable Skew, in Integer UI	-20 -20	UI UI	D-PHY, Lane to Lane C-PHY, Trio to Trio
Coarse Skew Range: Maximum Programmable Skew, in Integer UI	+20 +20	UI UI	D-PHY, Lane to Lane C-PHY, Trio to Trio
Coarse Skew Resolution 1.0 Gbps / 1.0 Gsps 9.0 Gbps / 6.5 Gsps	0.125 1.0	UI UI	D-PHY, Lane to Lane C-PHY, Trio to Trio
Fine Skew Range: Minimum Programmable Skew	-500 -500	ps ps	D-PHY, HS Clock to Data C-PHY, Wire to Wire Testing limit – hardware is capable of larger skews
Fine Skew Range: Maximum Programmable Skew	+500 +500	ps ps	D-PHY, HS Clock to Data C-PHY, Wire to Wire Testing limit – hardware is capable of larger skews
Fine Skew Injection Resolution	1	ps	D-PHY or C-PHY

TABLE 11: HS PATTERN HANDLING CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
User-Programmable Pattern Memory			
Minimum Pattern Segment Size	8	Bits	
Maximum Pattern Segment Size	8	GBytes	
Total Memory Space for Transmitters	8	GBytes	
Pattern Sequencer			
Sequence Control	Yes		Loop infinite Loop-on-count (see count below) Play to end
Number of Sequencer Slots per Pattern Generator	16		Each pattern generator can string up to 16 different segments together, each with its own repeat count
Number of Entry Slots	1		Separate from above 16 segments
Number of Exit Slots	1		Separate from above 16 segments
Maximum Repeat Count Per Slot	65536		
Maximum Repeat Count for Outer Loop	65536		Outer loop can encompass any number of slots
Additional Pattern Characteristics			
Escape Mode Command Entry	Yes		Per Lane
Pattern Switching	Yes		Wait to end of segment, or immediate

TABLE 3: GPIO AND I2C VOLTAGE CHARACTERISTICS

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	1.8	V	All GPIOs operate at 1.8 V LVCMOS
V _{IL} minimum	-0.3	V	
V _{IL} maximum	0.6	V	
V _{IH} minimum	1.2	V	
V _{IH} maximum	2.1	V	
V _{OL} maximum	0.45	V	
V _{OH} minimum	1.35	V	



REVISION NUMBER	HISTORY	DATE
1.0	Document release	July 27, 2020
1.1	Fixed error in the data rate specification	July 27, 2020
1.2	Updated D-PHY data rate specification	July 14, 2021
1.3	Updated specifications and added description of GPIO pinout and GPIO voltage specifications	April 11, 2022
1.4	Replaced Introspect ESP Software for Pinetree	July 26, 2023
1.5	Added embedded clock in table 4	November 16, 2023
1.6	Updated Logic Level Accuracy in Table 7	March 14, 2025
1.7	Updated specifications tables	March 17, 2025
1.8	Updated Figure 1; added temperature range & updated max current draw in Table 5; updated GPIO Connector Pinout and added Power Connector Pinout	November 26, 2025

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