



# DDR/LPDDR Protocol Analyzer

March 2026

# Introspect Makes Tools for Engineers

## ADDRESSING GAP IN TEST EQUIPMENT AVAILABILITY



~~Costly, few lanes, slow~~

- Bench-like accuracy and precision
- EDA style scripting
- Software-style regression and versioning

~~Rigid, low performance~~

- ATE-like speed
- Highly parallel
- Designed for automation

# We Test Electronic Interfaces...

**IR Range Finders**

**Image sensors**

**Motion sensors,  
microphones, speakers**

**Applications  
processors**



**Displays**

**Power  
management ICs**

**Memories**

**RF ICs**

# We Act as a Link Partner / Exerciser...



# And We Probe a Live System!



# The Products and Protocols at a Glance

## MIPI

CSI-2, DSI-2  
C-PHY, D-PHY, M-PHY  
Exercisers & Analyzers

## DISPLAYPORT

eDP and DP  
USB Type-C Alt-Mode  
Exercisers & Analyzers

## DDR MEMORY

LPDDR, DDR, GDDR  
Exercisers & Analyzers

## DIGITAL IO

I2C, I3C, SPI, SoundWire,  
SWI3S Exercisers &  
Analyzers

## PARALLEL BERT SOLUTIONS AND MISCELLANEOUS PROTOCOLS

OLDI, SLVS-EC, Vx1 HS, PCIe, USB 4, ONFI

## PROBES AND INTERPOSERS

Parallel, Active Probes Up to 35 GHz, Interposers, Solder-Down Tips

# The Products and Protocols at a Glance

## MIPI

CSI-2, DSI-2  
C-PHY, D-PHY, M-PHY  
Exercisers & Analyzers

## DISPLAYPORT

eDP and DP  
USB Type-C Alt-Mode  
Exercisers & Analyzers

## DDR MEMORY

LPDDR, DDR, GDDR  
Exercisers & Analyzers

## DIGITAL IO

I2C, I3C, SPI, SoundWire,  
SWI3S Exercisers &  
Analyzers

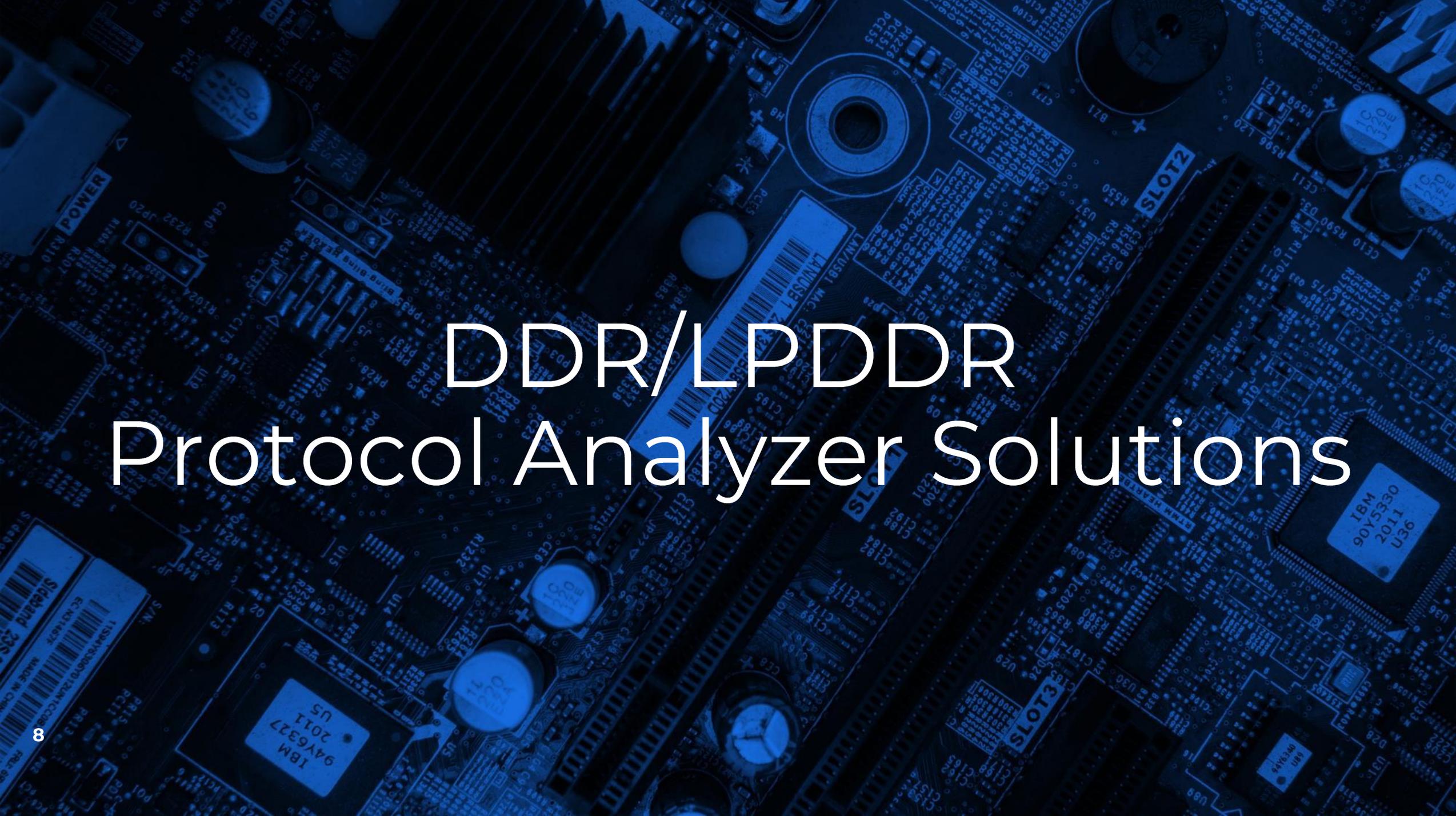
## PARALLEL BERT SOLUTIONS AND MISCELLANEOUS PROTOCOLS

OLDI, SLVS-EC, V

## PROBES A

Parallel, Active Probes Up to 3

**Focus of This  
Presentation**



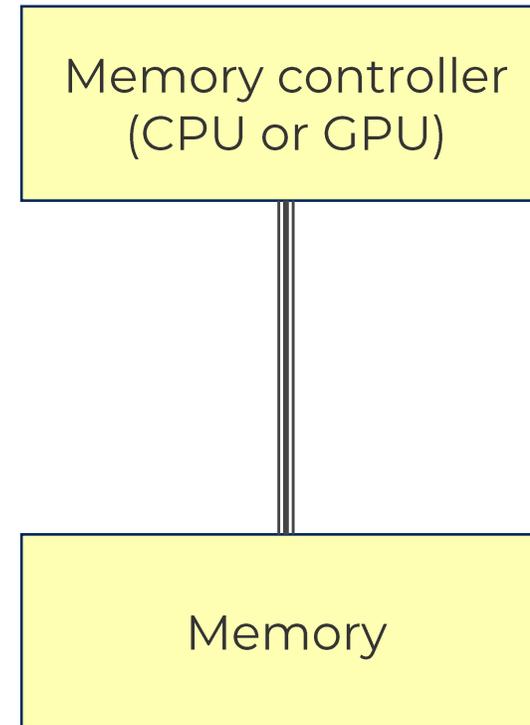
# DDR/LPDDR Protocol Analyzer Solutions

# Problem Statement: Debugging a Live System

## COMMUNICATION IS HARD

- Separate companies design and manufacture the controllers and memories
- Difficult to understand what exactly the other party is doing
- A design that works in simulation or prototyping often fails to perform adequately in a live system

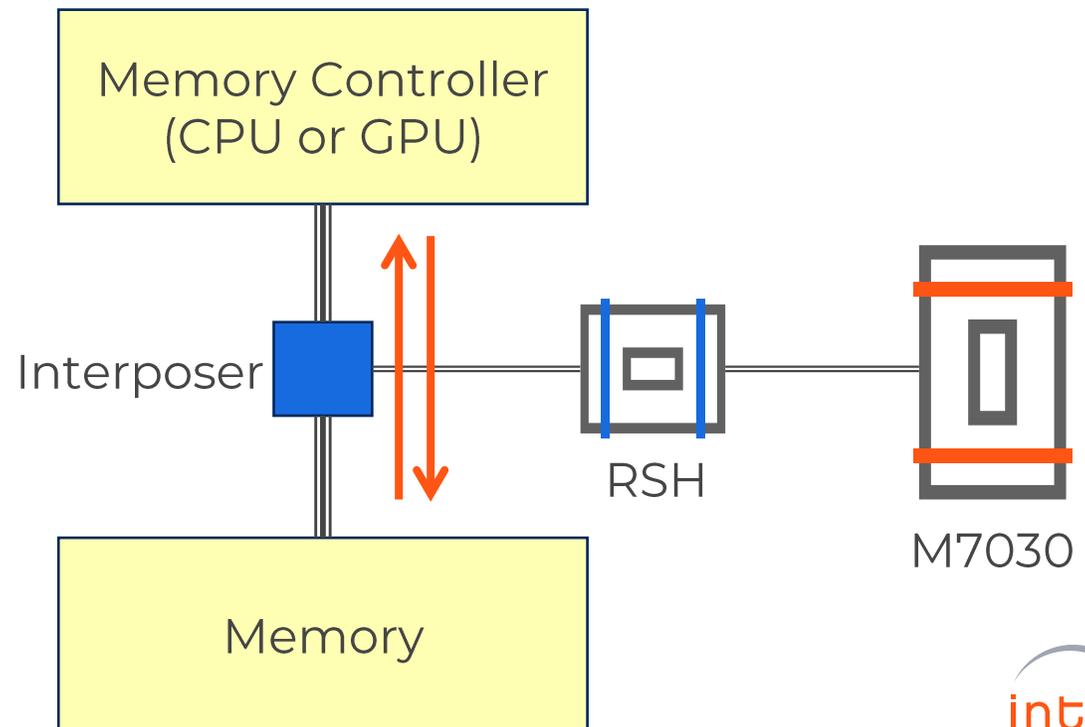
**Question:** How do you approach debugging a poorly performing DDR system?



# Analyzer Concept

## DDR/LPDDR LINK SNIFFER

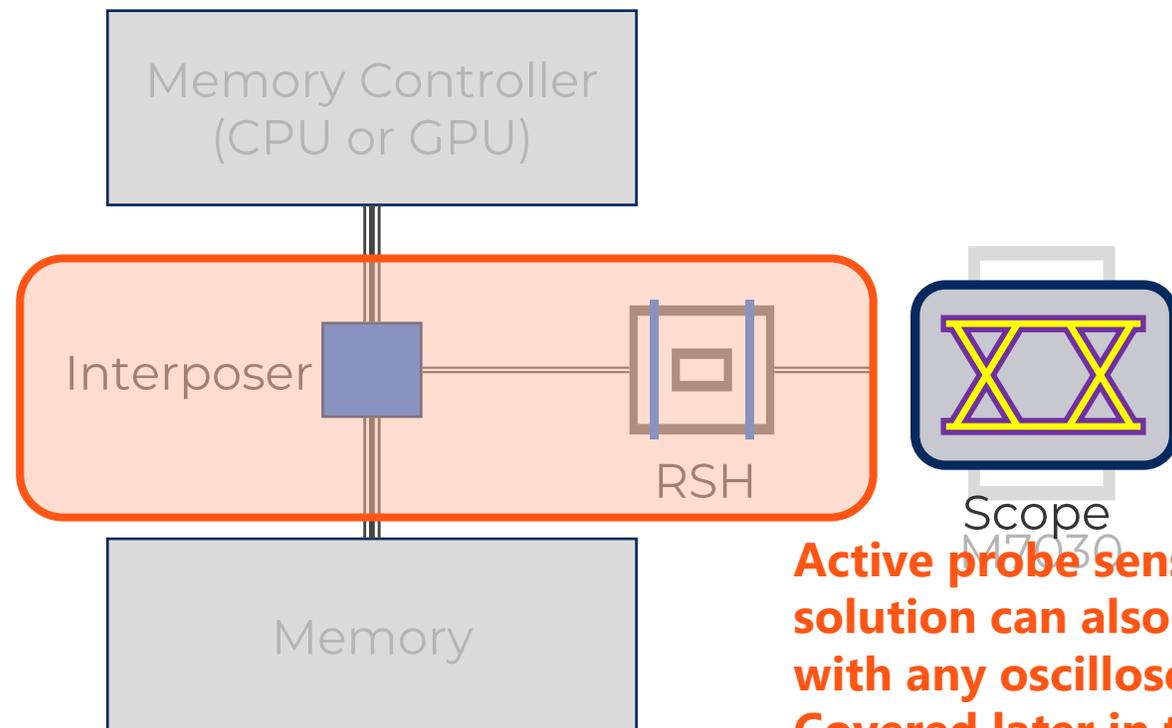
- Not a source, not a sink
- **Active probes** do not degrade the signal; the controller and memory can communicate normally



# Analyzer Concept

## DDR/LPDDR LINK SNIFFER

- Not a source, not a sink
- **Active probes** do not degrade the signal; the controller and memory can communicate normally

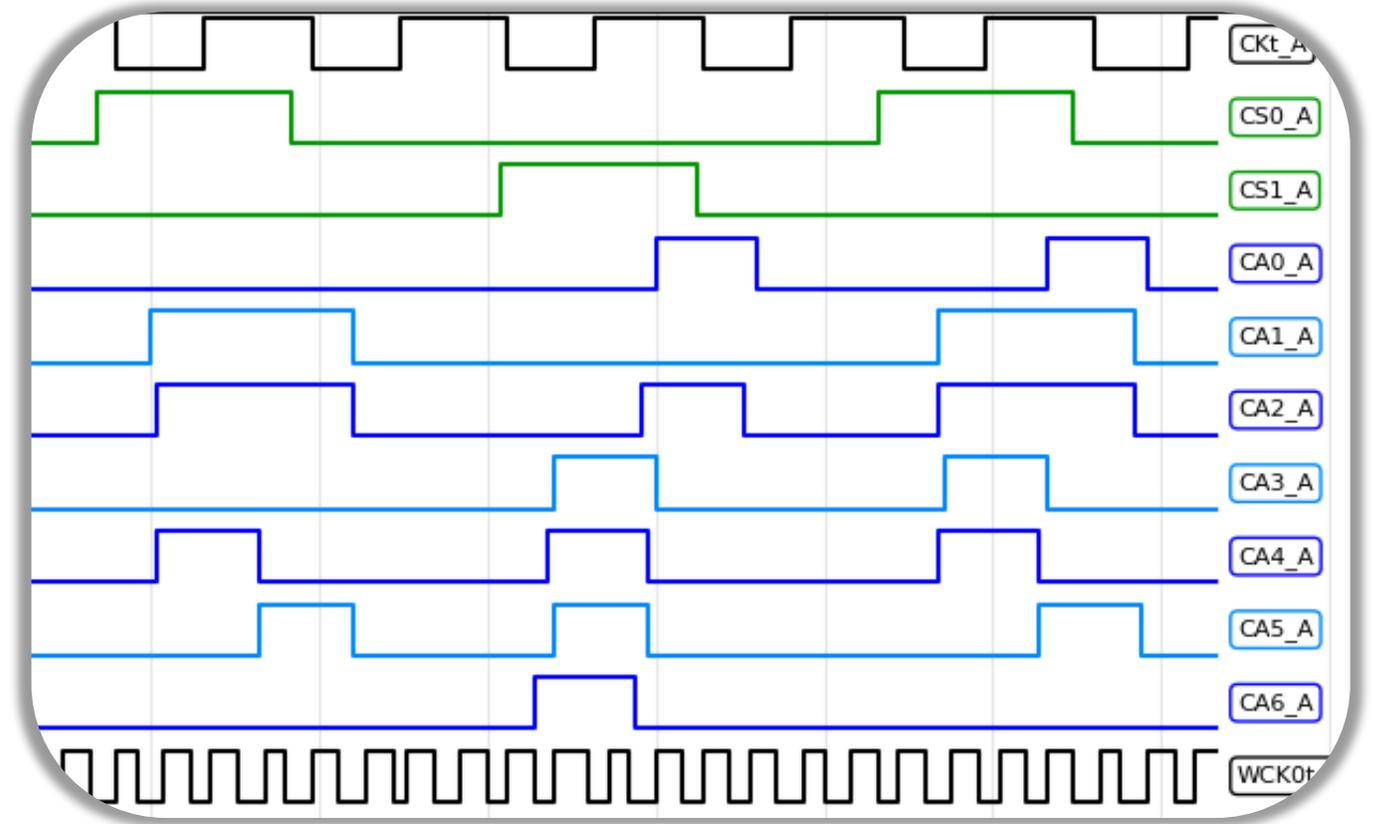
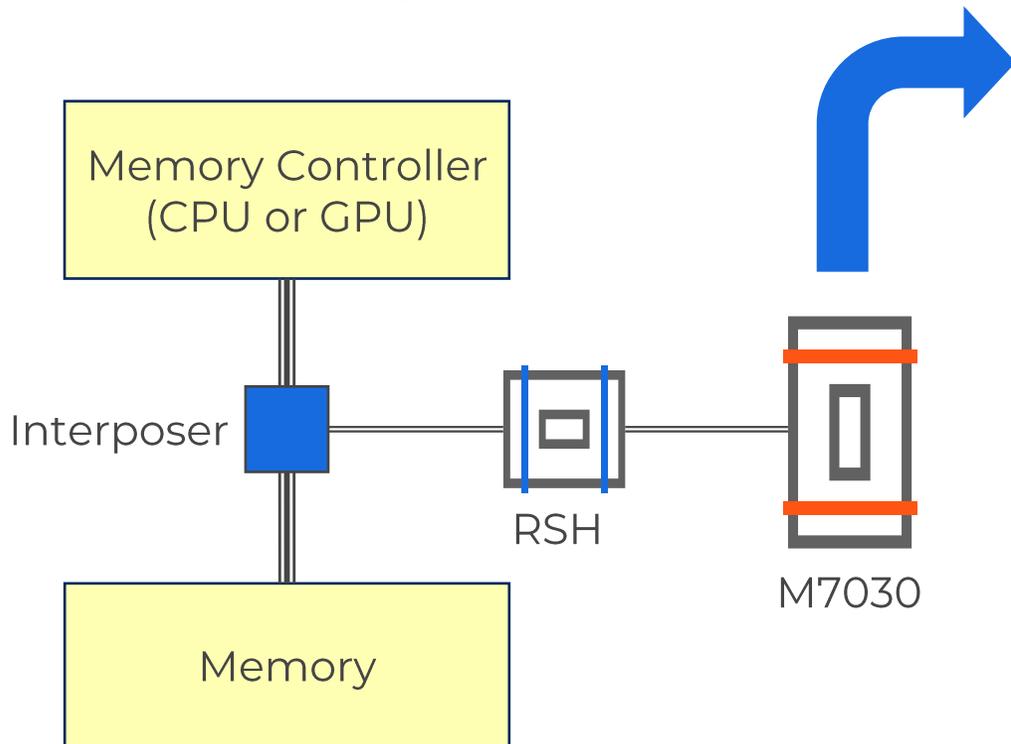


**Active probe sensing solution can also be used with any oscilloscope. Covered later in this presentation.**

# Capture DDR/LPDDR Signals

## ALIGNED PARALLEL CAPTURE

- Capture logical signals on Command and Data channels
- Up to 36 aligned channels

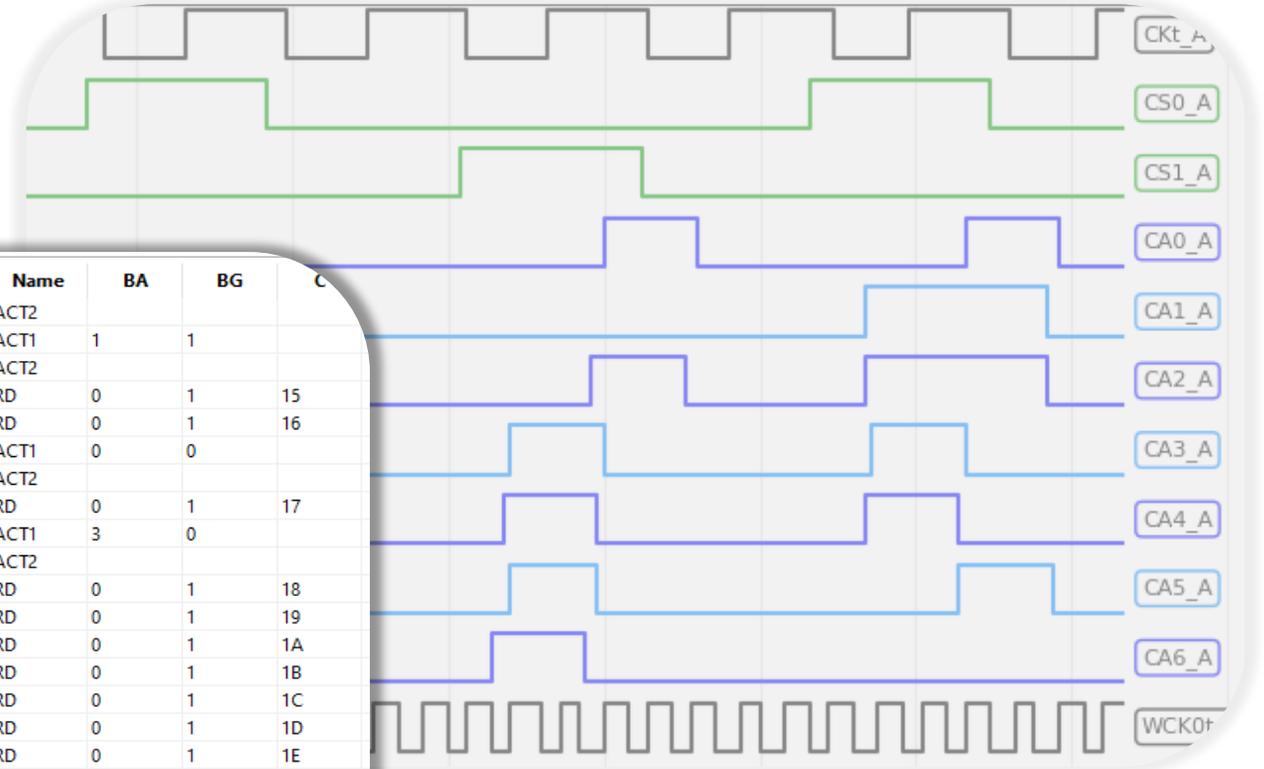


Captured logical signals of the DDR command bus

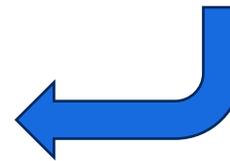
# High Level Analysis

## COMMAND DECODING

Interpret logical signals into DDR commands



Cmd#	Time (µs)	Time (nCK)	CK Freq (MHz)	WCK Rate (Mbps)	Burst#	Name	BA	BG	C
160	0.774	460	599.0			ACT2			
161	0.776	461	599.0			ACT1	1	1	
162	0.778	462	599.0			ACT2			
163	0.779	463	599.0	4719.0		RD	0	1	15
164	0.786	467	599.0	4719.0		RD	0	1	16
165	0.787	468	599.0			ACT1	0	0	
166	0.789	469	599.0			ACT2			
167	0.793	471	599.0	4719.0		RD	0	1	17
168	0.798	474	599.0			ACT1	3	0	
169	0.799	475	599.0			ACT2			
170	0.801	476	599.0	4719.0		RD	0	1	18
171	0.808	480	599.0	4800.0		RD	0	1	19
172	0.814	484	599.0	4800.0		RD	0	1	1A
173	0.821	488	599.0	4800.0		RD	0	1	1B
174	0.828	492	599.0	4800.0		RD	0	1	1C
175	0.834	496	599.0	4800.0		RD	0	1	1D
176	0.841	500	599.0	4800.0		RD	0	1	1E
177	0.848	504	599.0	4800.0		RD	0	1	1F
178	0.859	511	599.0			PRE	0	1	
179	0.864	514	599.0	4800.0		WR	1	1	19
180	0.871	518	599.0	4800.0		WR	2	1	14
181	0.878	522	599.0	4800.0		WR	3	1	1B
182	0.879	523	599.0			ACT1	0	1	
	0.881	524	599.0			ACT2			



# High Level Analysis

## COMMAND DECODING

Interpret logical signals into DDR commands

The screenshot displays a protocol analyzer interface for command decoding. On the left, there is a 'Command Selection' section with 'Go To:' buttons for 'Prev', 'Next', and 'CAS'. Below this is the 'Command #383: Details' section, which includes the command name 'CAS', rank '0 1', and bits 'K CS CA23456', 'R 11 0011001', and 'F 01 0000000'. A 'Go to waveform' button is also present. To the right of the details is a table of arguments and values:

Argument	Value
DC	0
WRX	0
WS_FS	1
WS_RD	0
WS_WR	0
WXSA	0
WXSB	0

At the bottom left, the 'Command #383: Timings' section shows 'No data is available.' On the right side of the interface is a large table listing decoded DDR commands:

Cmd#	Time (μs)	Time (nCK)	CK Freq (MHz)	WCK Rate (Mbps)	Burst#	Name
376	50684.966	15117363	599.0			NOP
377	50684.968	15117364	599.0			REF
378	50684.969	15117365	599.0			NOP
379	50684.990	15117377	599.0			PDE
380	50685.252	15117534	599.0			PDX
381	50685.252	15117535	599.0			NOP
382	50685.276	15117549	599.0			MPC
383	50685.311	15117570	599.0			CAS
384	50685.313	15117571	599.0			MRR
385	50685.333	15117583	599.0			MRR
386	50685.353	15117595	599.0			MPC
387	50685.375	15117608	599.0			MPC
388	50685.396	15117621	599.0			CAS
389	50685.410	15117629	599.0			REF

Main view of decoded DDR commands in the protocol analyzer viewer

# High Level Analysis

## COMMAND ANALYSIS

- Compute and validate the timing symbols relevant to each command
- Navigate quickly to out-of-spec timings via search and/or highlighting in the command list
- Validate command sequencing is correct (not shown)

The screenshot displays a software interface for command analysis. At the top, there is a 'Command Selection' section with 'Go To:' buttons for 'Prev', 'Next', and a dropdown menu set to 'Timing Violation'. Below this is the 'Command #121: Details' section, which includes the command name 'WR', rank '0', and bits 'K CS CA23456', 'R 10 0110000', and 'F 00 0110110'. A table lists arguments and their values: AP (0), BA (2), BG (1), and C (6). A 'Go to waveform' button is located below the details. The 'Command #121: Timings' section features a link to 'View Timing Definitions' and a table of timing parameters.

Reference Command	Value	Min	Max	Unit	Symbol
122 (RD)	10.00	2.00	-	nCK	tWTRcr_16
132 (PRE)	39.00	49.00	-	nCK	WL+BL_min+1+nWR
179 (WR)	148.00	2.00	-	nCK	tWTWcr_16
199 (WR)	239.00	4.00	-	nCK	BL

Measured timings (bottom) for a write command. The timing relative to the “PRE” command is slightly too short, according to the LPDDR specification

# High Level Analysis

## MODE REGISTER DECODING

- Interpret mode register transmissions for easy review
- Specific decoding for each mode register

Command #44: Mode register

Addr	Bit	Entry	Val	Detail
12h	2:0	WCK_ODT	011b	RZQ/3
12h	3	WCK_FM	1b	High frequency mode
12h	4	WCK_ON	1b	WCK Always On Mode enabled
12h	5	RFU	0b	
12h	6	WCK2CK_LEVELING	0b	
12h	7	CKR	0b	4:1 ratio

Decoding of Mode Register 12h

Command #2: Details

Name: MRW2  
Rank: 0  
Bits:  
K CS CA23456  
R 10 0001000  
F 00 1000001

Argument	Value
OP	41

Go to waveform

Command #2: Mode register

Addr	Bit	Entry	Val	Detail
10h	1:0	FSP_WR	01b	Frequency-Set-Point [1]
10h	3:2	FSP_OP	00b	Frequency-Set-Point [0] (default)
10h	5:4	CBT	00b	Normal Operation (default)
10h	6	VRCG	1b	VREF Fast Response (high current) mode
10h	7	CBT_PHASE	0b	DQ outputs CA latched by CK rising edge (default)

Decoding of Mode Register 10h  
Opcode 41h was decoded in 5 separate entries, specific to address 10h

# Clock Changes? No Problem!

## ANY CLOCK GOES

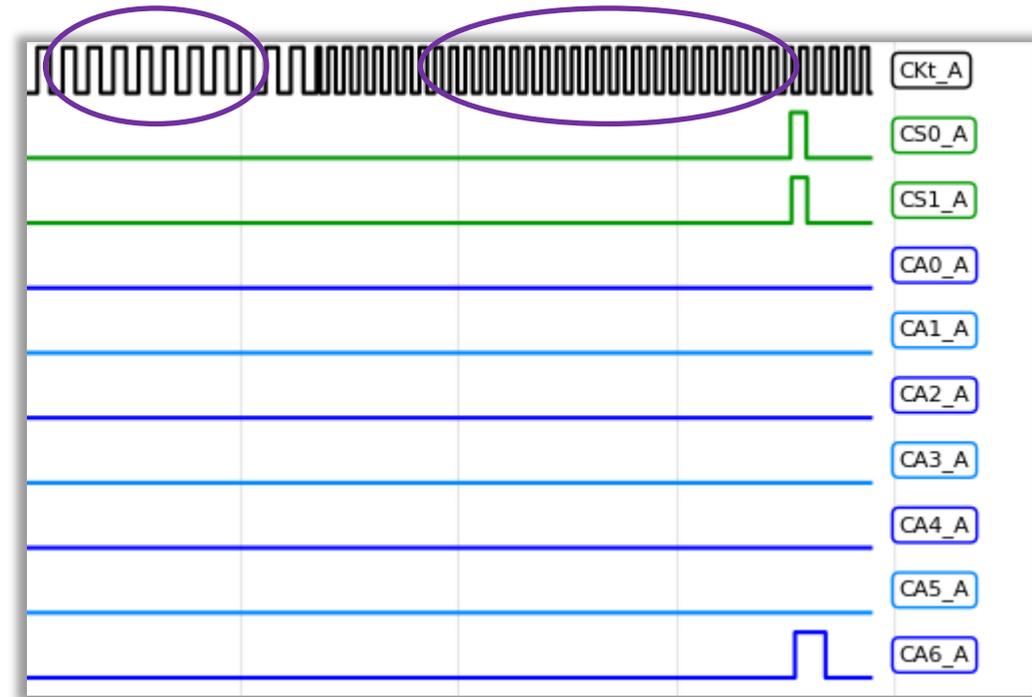
- The Protocol Analyzer is designed from the ground up to gracefully handle quick clock frequency changes
- It is not synchronized to a clock signal from the controller

Cmd#	Time (μs)	Time (nCK)	CK Freq (MHz)	WCK Rate (M)
85	1725.286	517566	300.0	
86	1725.304	517571	300.0	
87	2668.495	800528	300.0	
88	2668.498	800529	300.0	
89	13420.086	0	498.0	
90	15625.041	1104560	498.0	
91	15625.043	1104561	498.0	
92	15797.542	1190356	498.0	

Clock changes shown in commands tab

Note: this resets the timestamp expressed nCK

**Note:** Instantaneous frequency change is tracked.



Clock change as observed in the logical signals

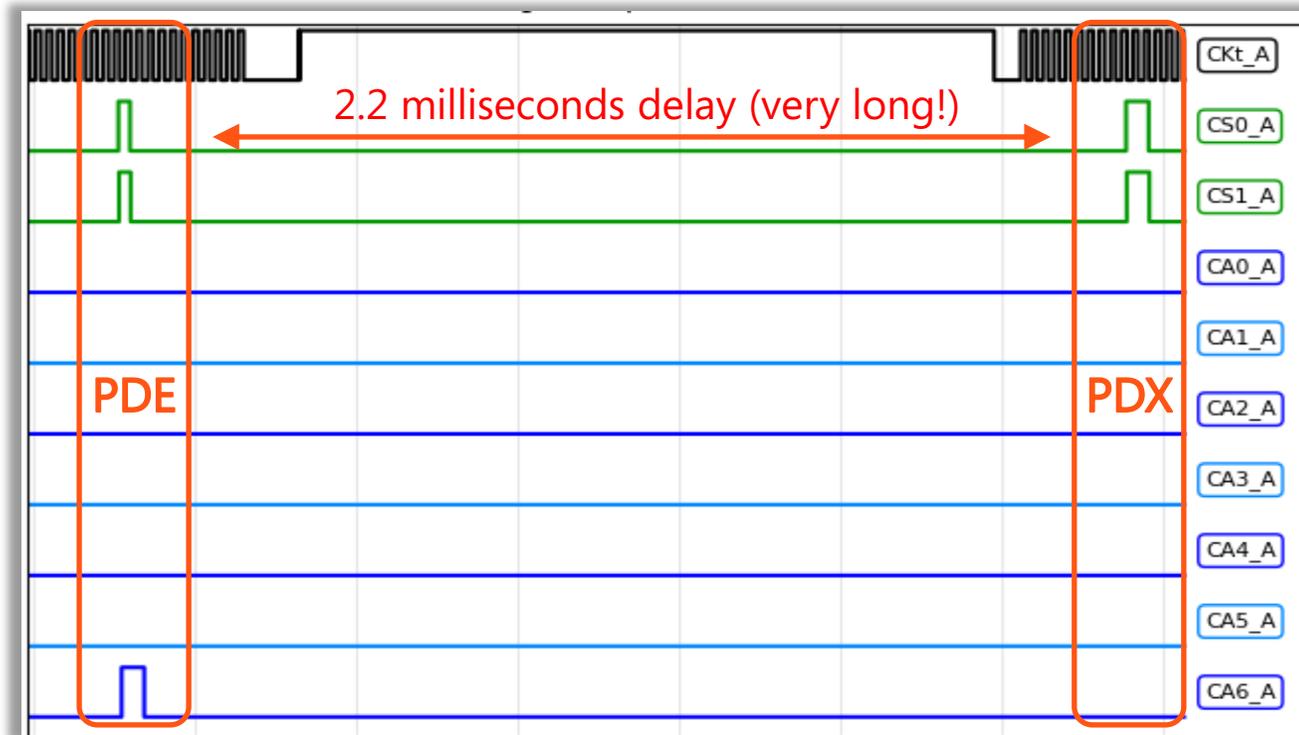
# Clock Stops? No Problem!

Note: timestamps show how long the clock stopped

## ANY CLOCK GOES, INCLUDING NONE

- Memory controllers often powers down the memory to save power
- The clock stops in this case
- Protocol Analyzer is not synchronized to clock: it tolerates prolonged clock stoppage without issues

Cmd#	Time (μs)	Time (nCK)	CK Freq (MHz)	WCK Rate (Mbps)	Burst#	Name
89	13420.086	0	498.0			PDE
90	15625.041	1104560	498.0			PDX

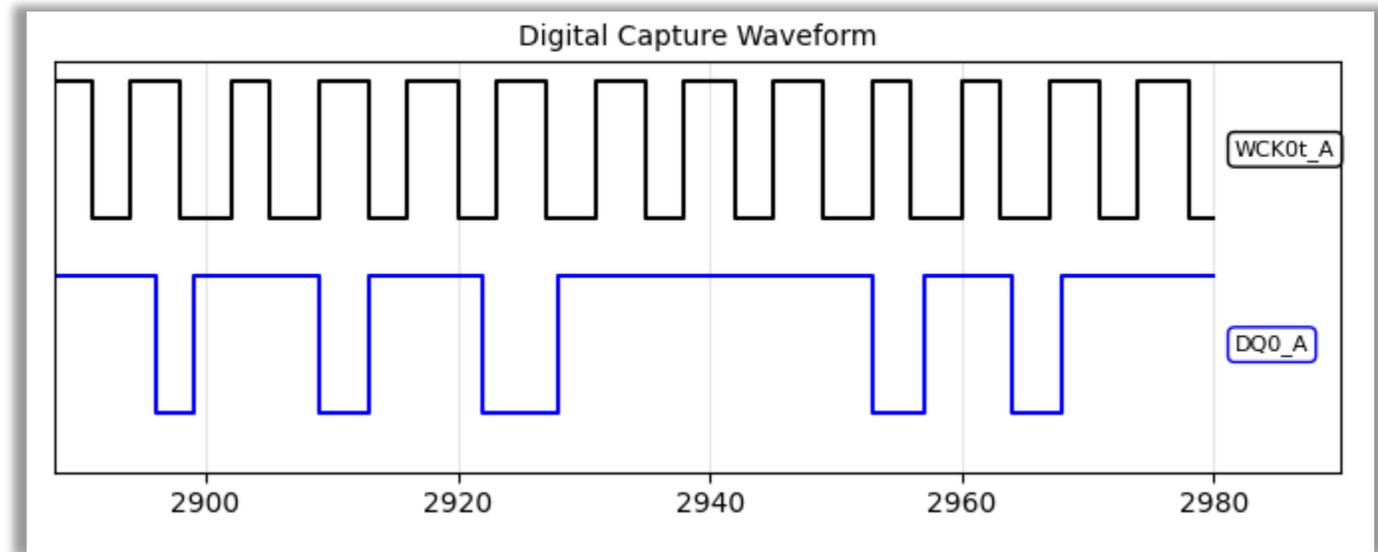


Example long clock stoppage during memory power down

# What about the data bus?

## SOURCE-SYNCHRONOUS SAMPLING

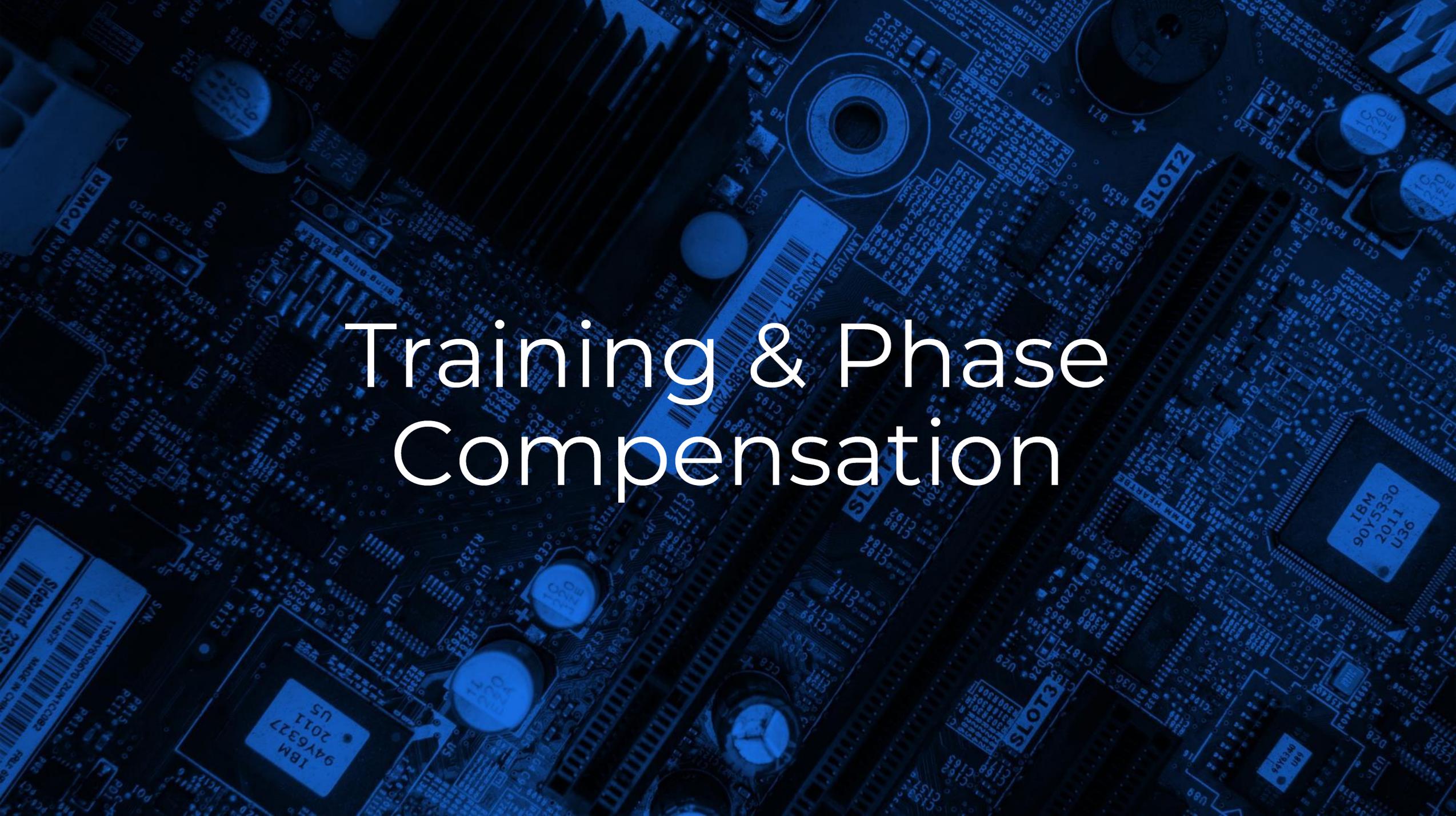
- Logic signals are captured at 80 Gbps (asynchronous sampling)
- We also *sample* the DQ with the clock (i.e. extract burst data). Requires DQ calibration on live traffic to estimate the write latency (not shown)



Example logical DQ data.

## PROBING LOCATION MATTERS

- Reflections can exist depending on where you probe
- See later section for guidance on probing locations



# Training & Phase Compensation

# No Training Needed!

## DDR TRAINING: FOR MEMORIES

- Complex sequence of operation for the controller and the memory to agree on many communication parameters (speed grade, phase, voltage reference, etc)
- On integrated systems, it is only done once. Training values are reused on next controller/memory bootup

## LIVE TRAFFIC PHASE COMPENSATION: FOR PROTOCOL ANALYZER

- Helps obtain accurate capture data in high-throughput conditions
- Done purely on live traffic. No need to set the controller in training mode
- Only necessary for very high-speed transmissions. Medium and low-speed transmissions (such as at startup) need minimal compensation for data to be acquired correctly

**Takeaway:** Introspect's DDR Protocol Analyzer does *not* need conventional DDR training

# Live Traffic Calibration

## VREF CALIBRATION

- DDR is single-ended. Need to determine reference voltage for accurate sampling
- Rapid algorithm that is executed once in Python

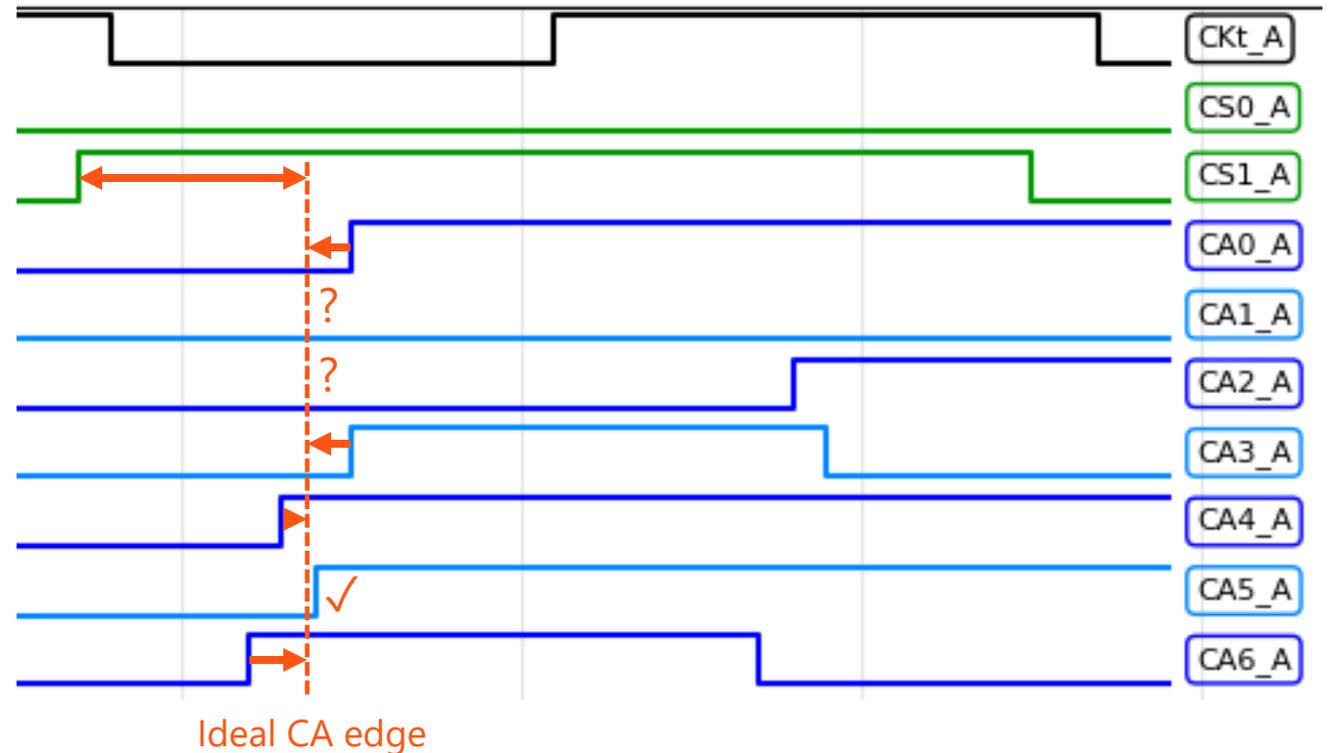
## CMD PHASE COMPENSATION

- Controller and memory may agree on large phases during training (more than one clock cycle off), making direct sampling with CK edges incorrect
- Need to determine where the ideal CA sampling point should be

# Live Traffic Compensation: CMD phase

## COMPENSATION IN ACTION

- Statistical in nature: Requires a lot of “random enough” data to correctly identify the ideal sampling point for *all* wires
- Supported for DDR5 and LPDDR5
- Only needed for high speeds. Low speeds (such as bootup captures) don't need phase calibration



Phase calibration in action (LPDDR5). Note that CA1 and CA2 phase cannot be determined here

# Target Audience

# Who can use the DDR PA?

## MEMORY MAKERS

- To prototype their in-house test fixtures
- To validate an external memory controller is within specification

## CPU COMPANIES

- To cross-check the output of their own controller when connected to an actual memory
- To validate their controller is within specification

## SYSTEM INTEGRATORS

- Understand why memories from different vendors perform differently
- Understand why a single CPU/Memory unit is faulty

# When to use the DDR PA?

## PROTOTYPING

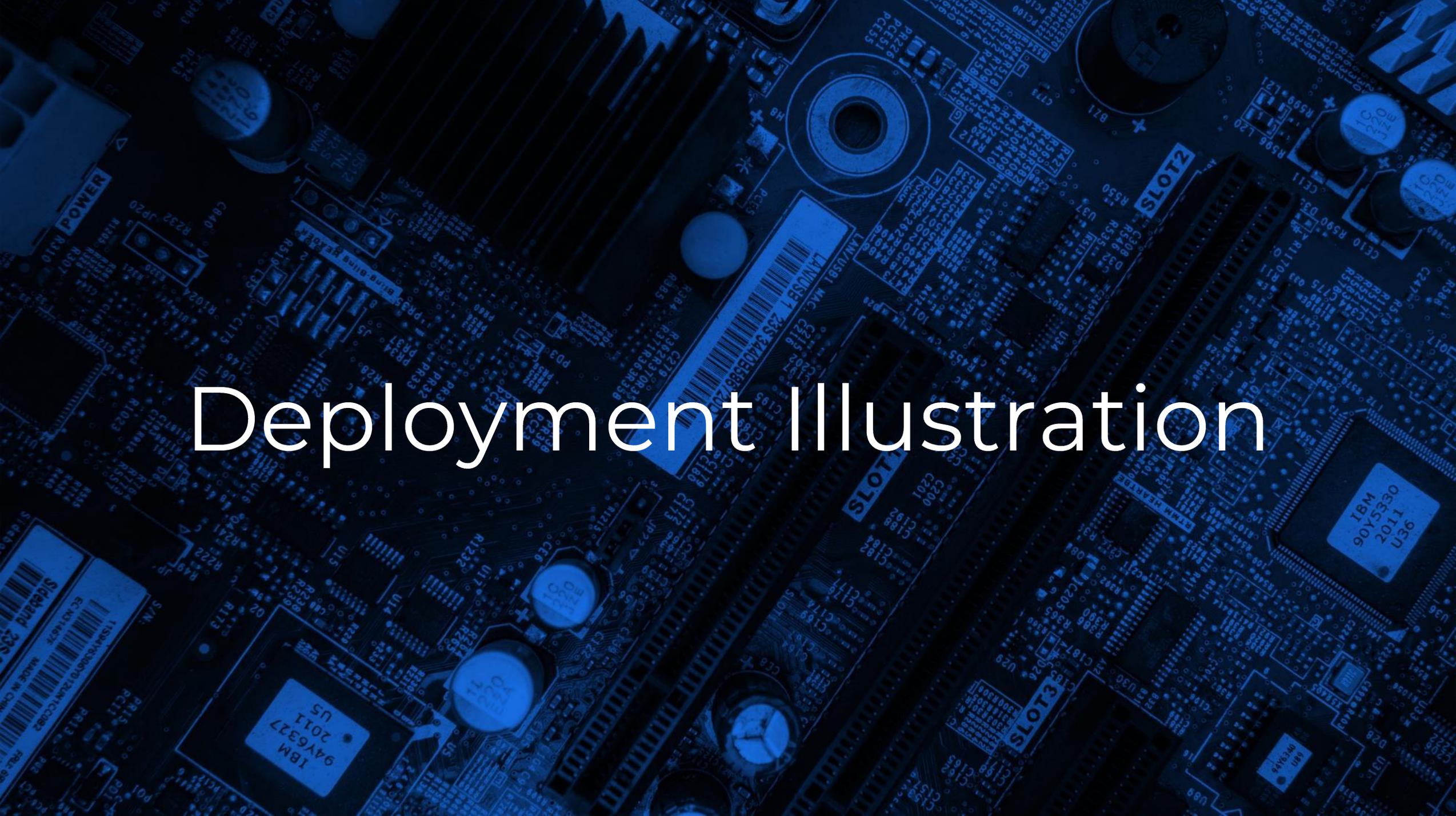
- Allows CPU companies to observe the output their own design
- Helpful to design internal test fixtures

## VALIDATION

- Understand compatibility issues with counterparties
- Decipher behaviour of low-probability error events

## PRODUCTION

- Determine why a CPU/Memory unit is faulty directly from the production line



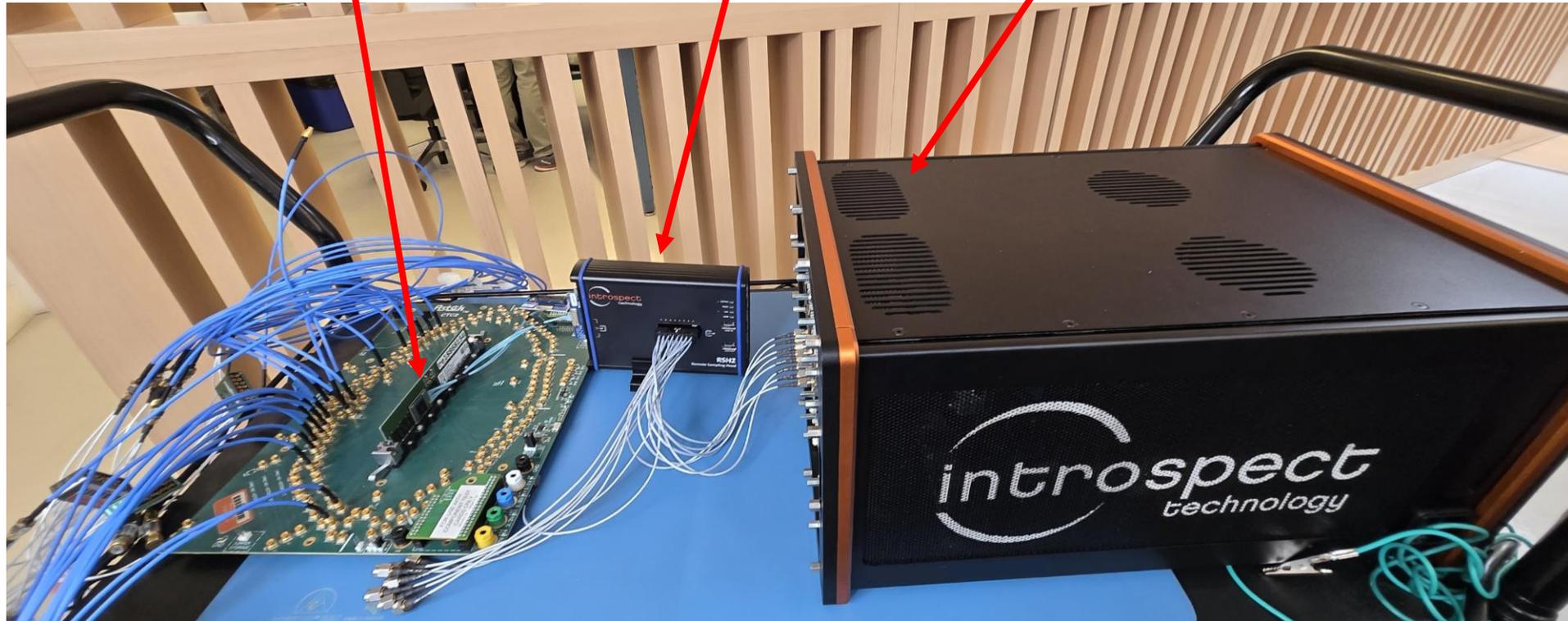
# Deployment Illustration

# Entire Bench Illustration

Interposer

RSH

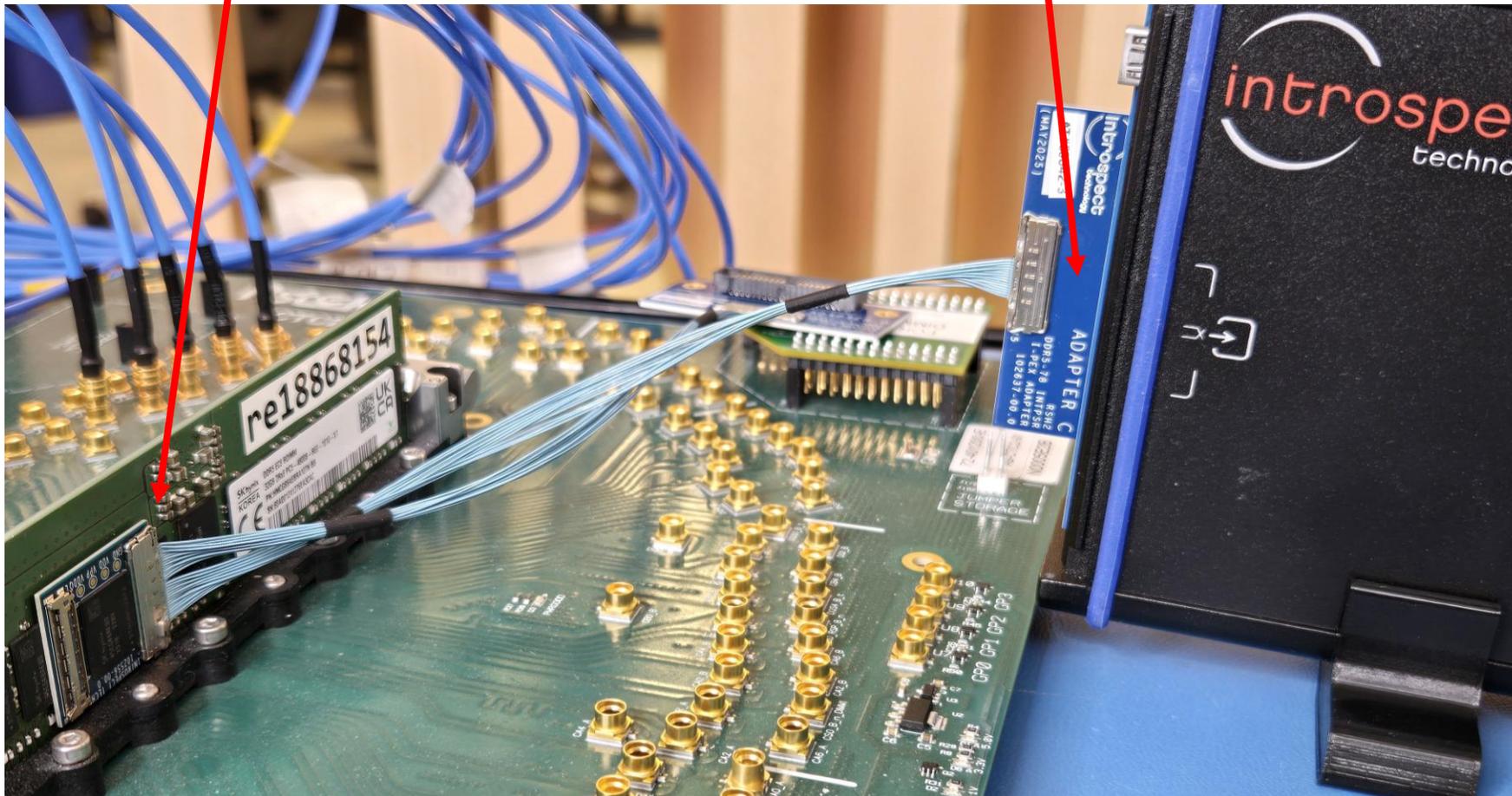
Analyzer



# Focus on Interposer

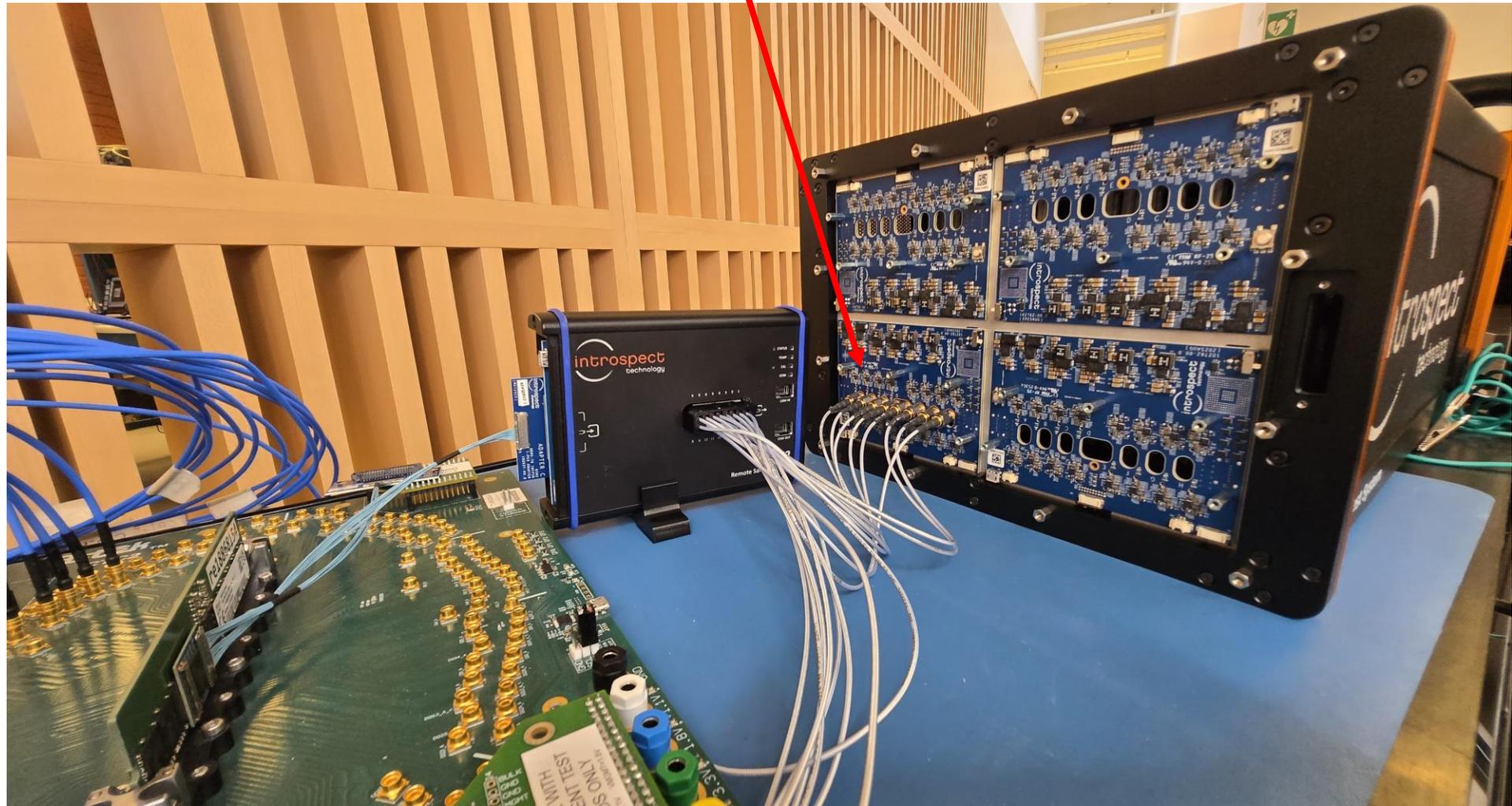
Shielded cables result in high signal integrity

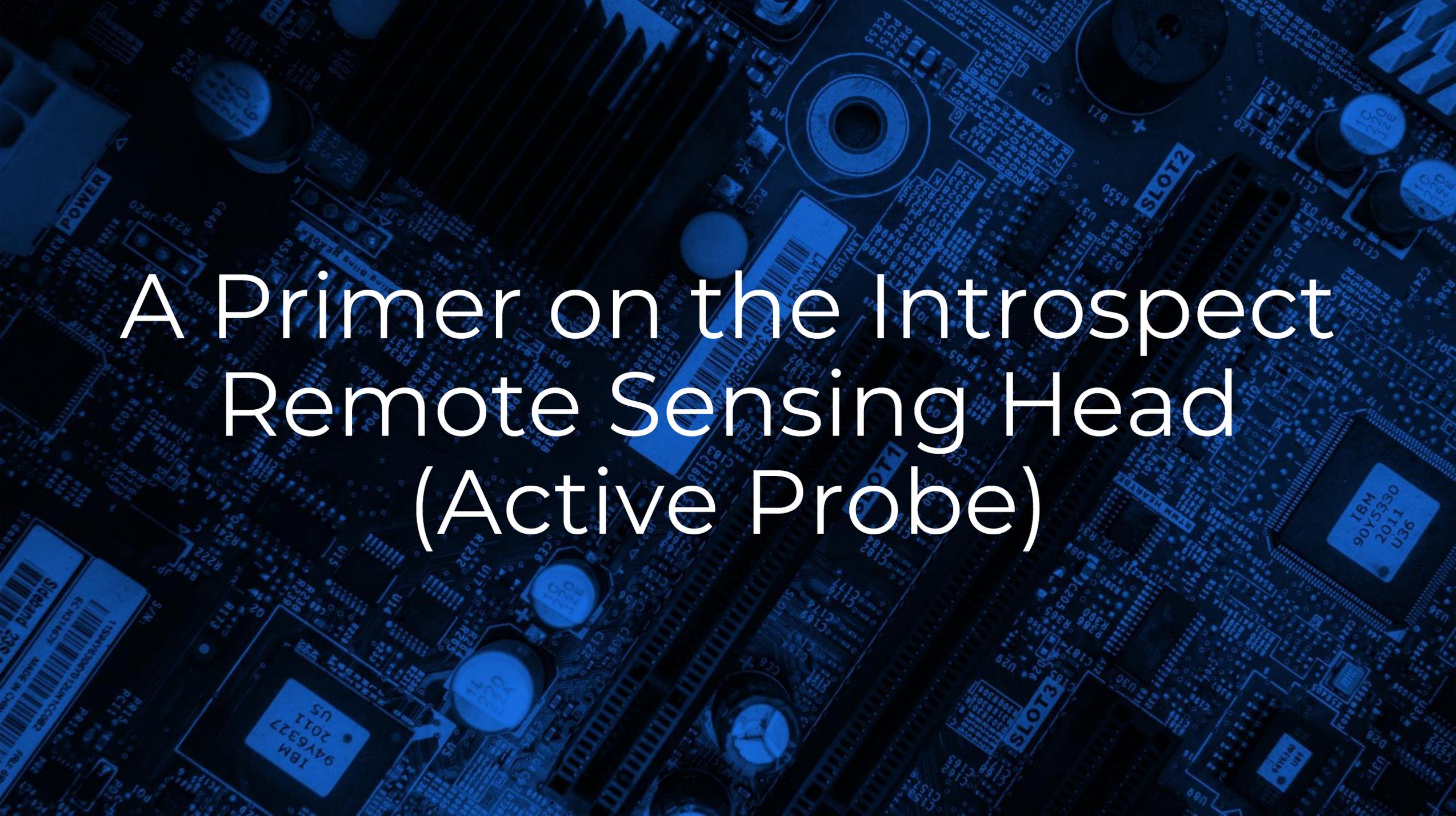
Interchangeable adapters for the probe amplifier (RSH)



# Focus on Analyzer Input

High-performance SMPM interface

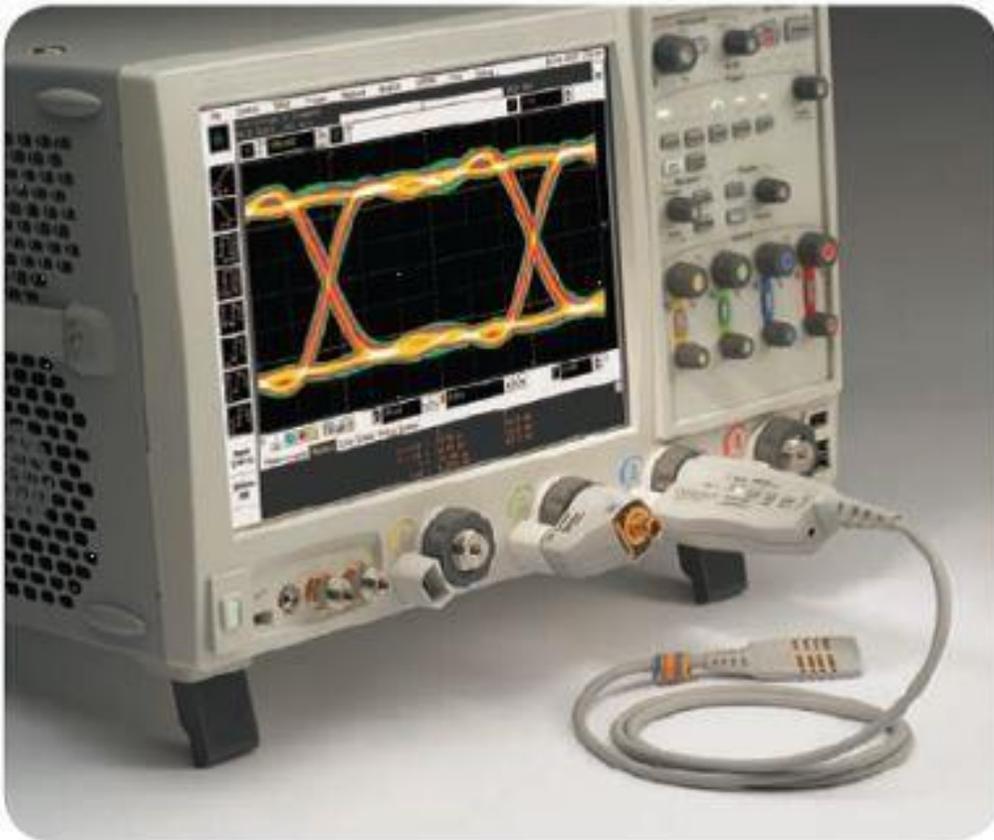




# A Primer on the Introspect Remote Sensing Head (Active Probe)

# Oscilloscope Probes

**PROPRIETARY TO SCOPE VENDOR**



# Oscilloscope Probe Anatomy

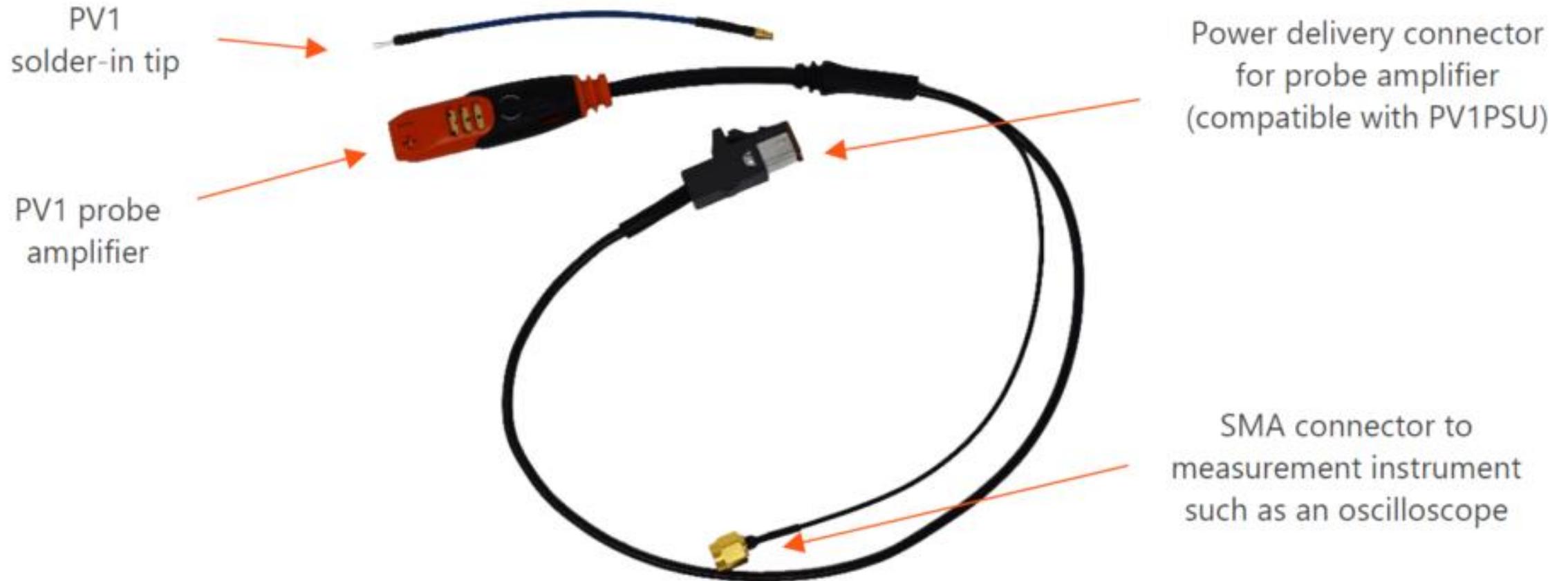


Solder-In Tip



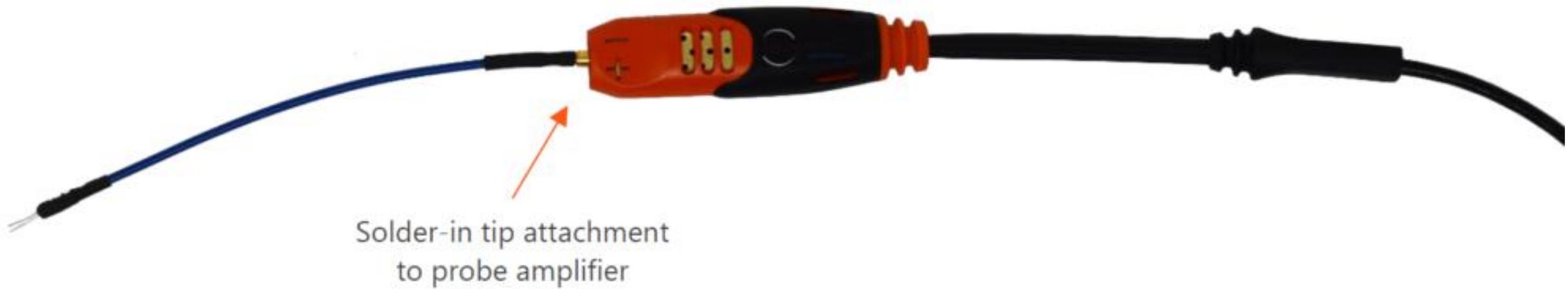
# Introspect's Probes

**COMPATIBLE WITH ANY SCOPE**

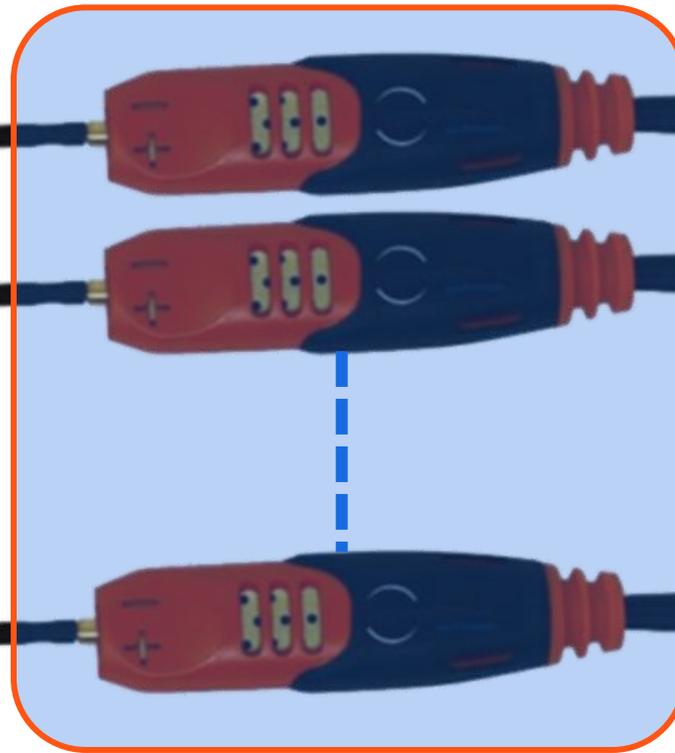


# Introspect's Probes

Tip is specifically designed for Introspect probe amplifier

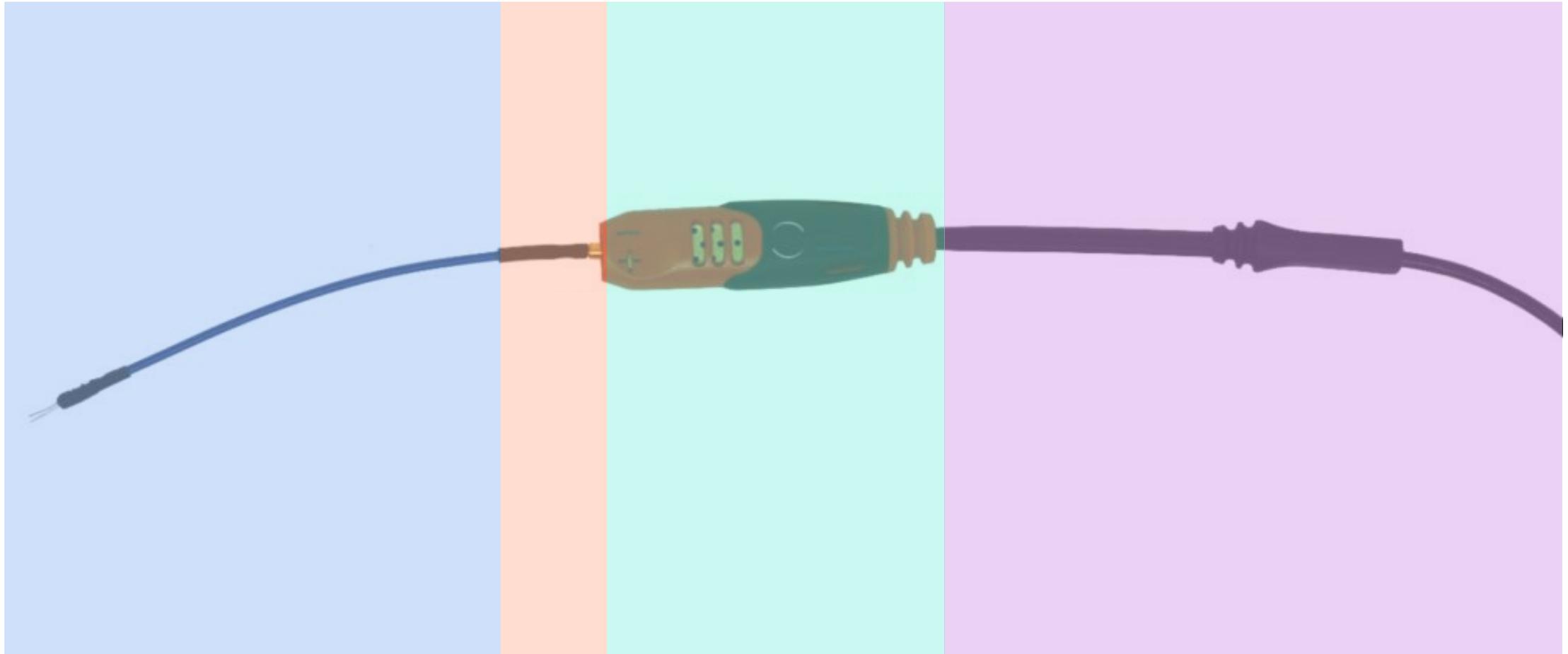


# RSH Is a Box Containing 12 Probes

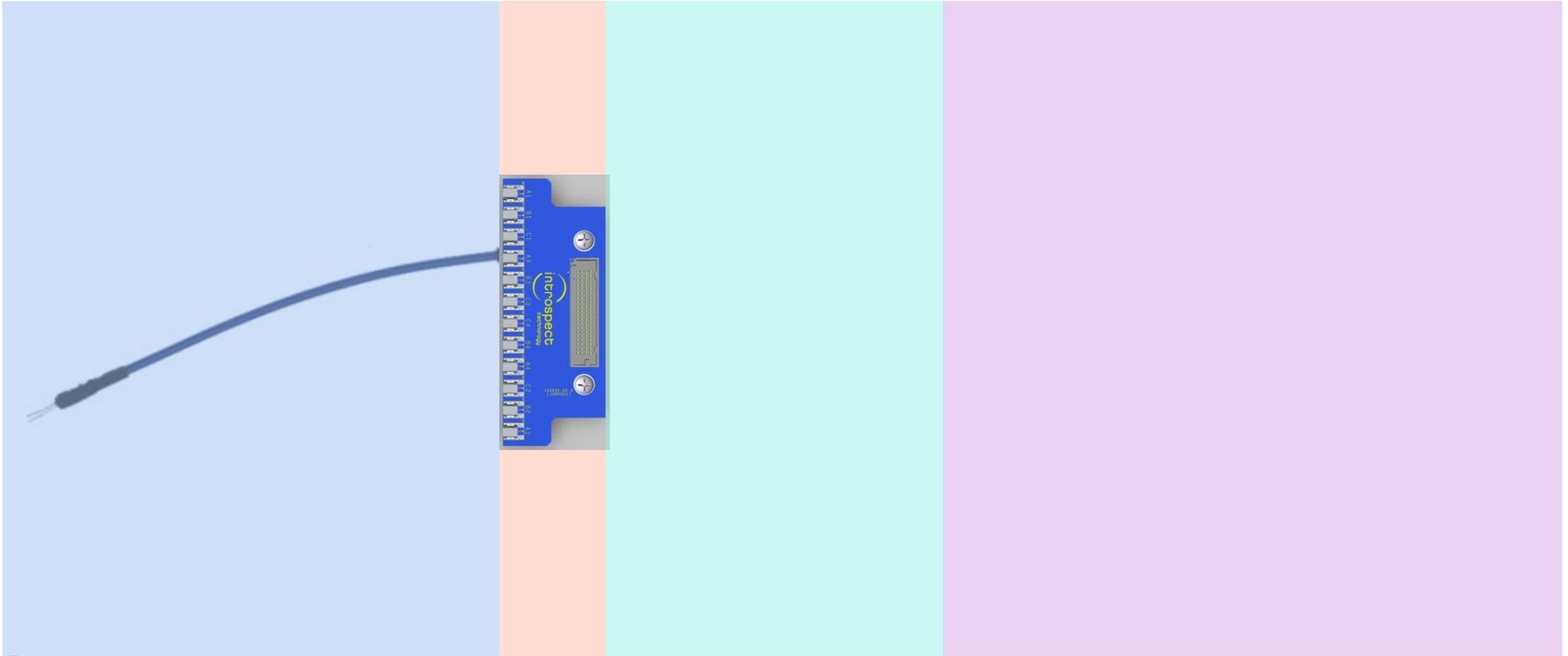


**INTROSPECT RSH**

# Evolution From Individual Probes



# Evolution From Individual Probes



38

**SOLDER TIP**

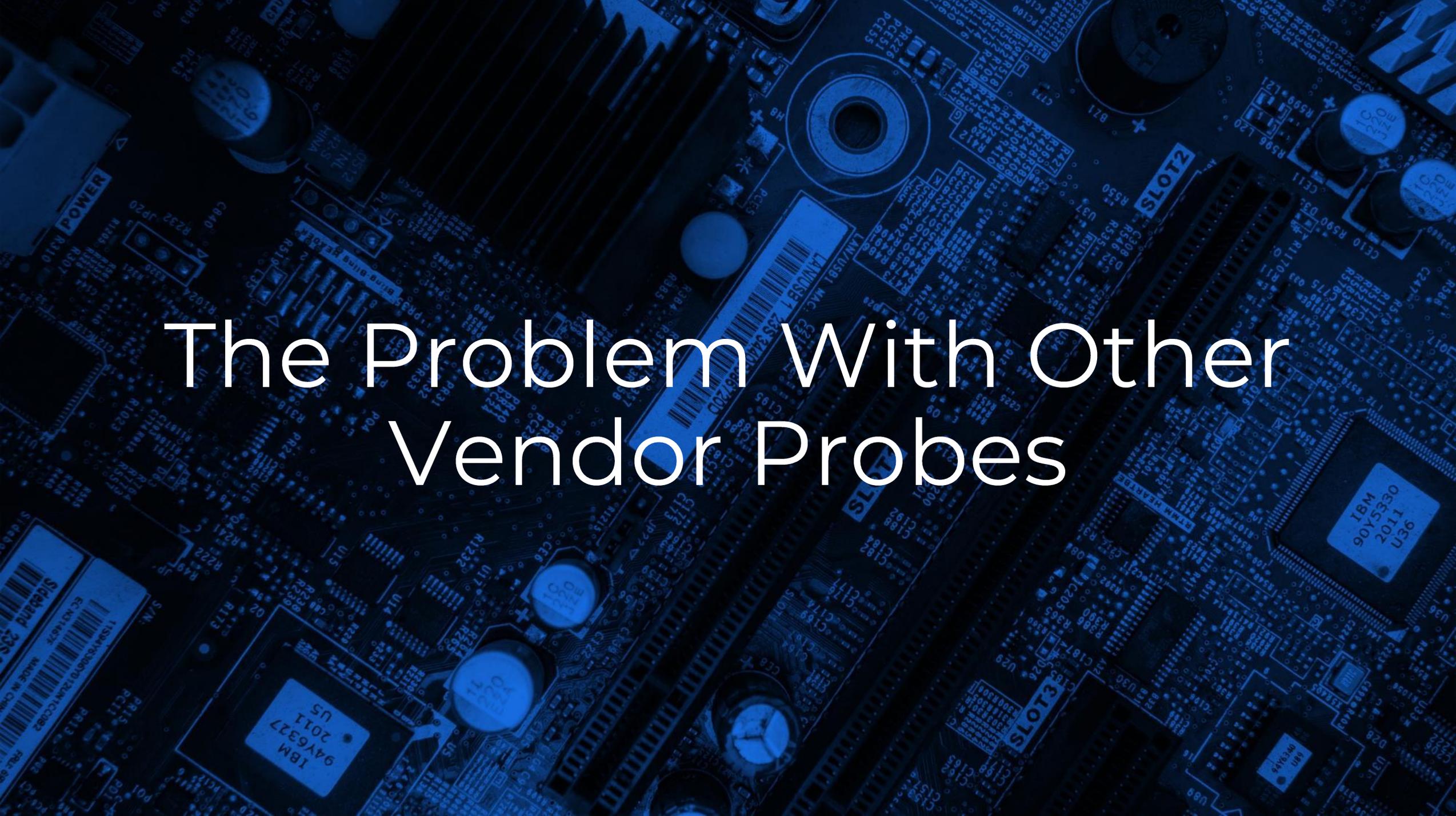
**TIP  
ATTACHMENT**

# Evolution From Individual Probes



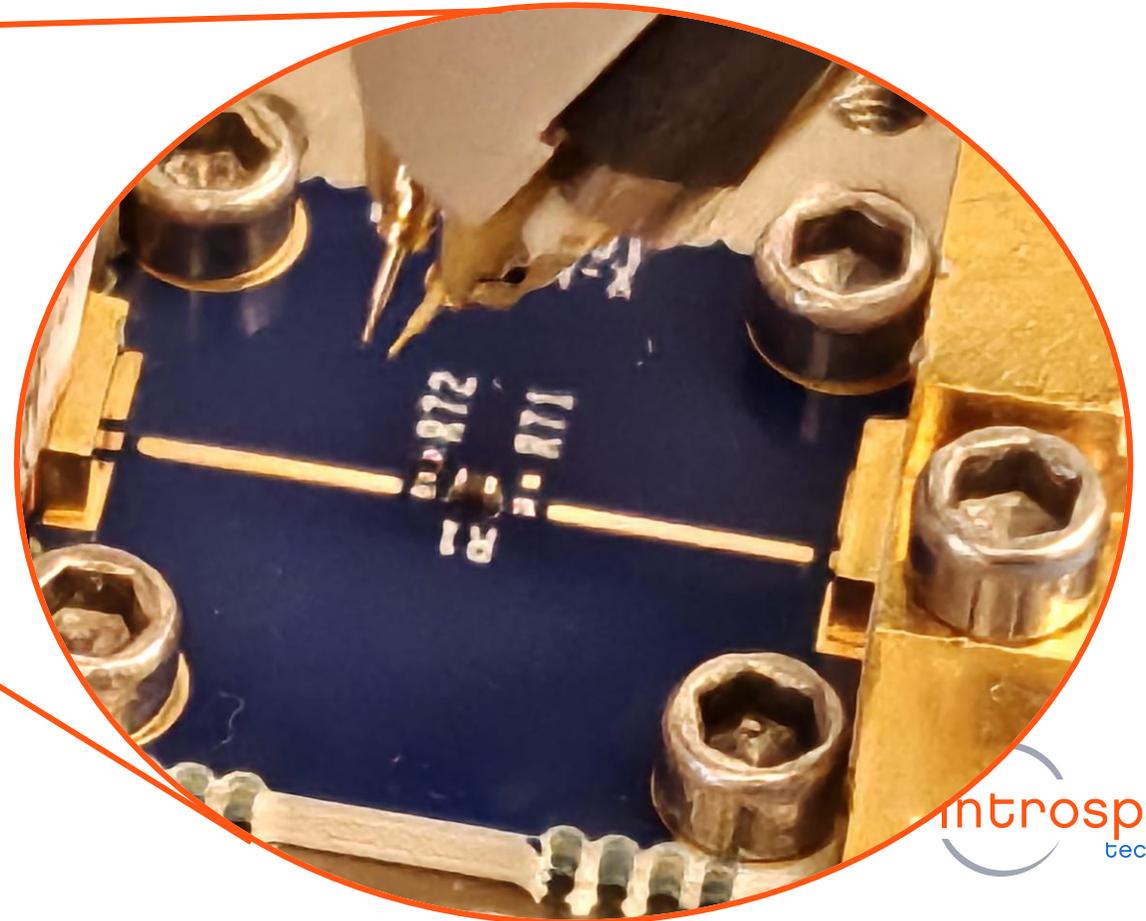
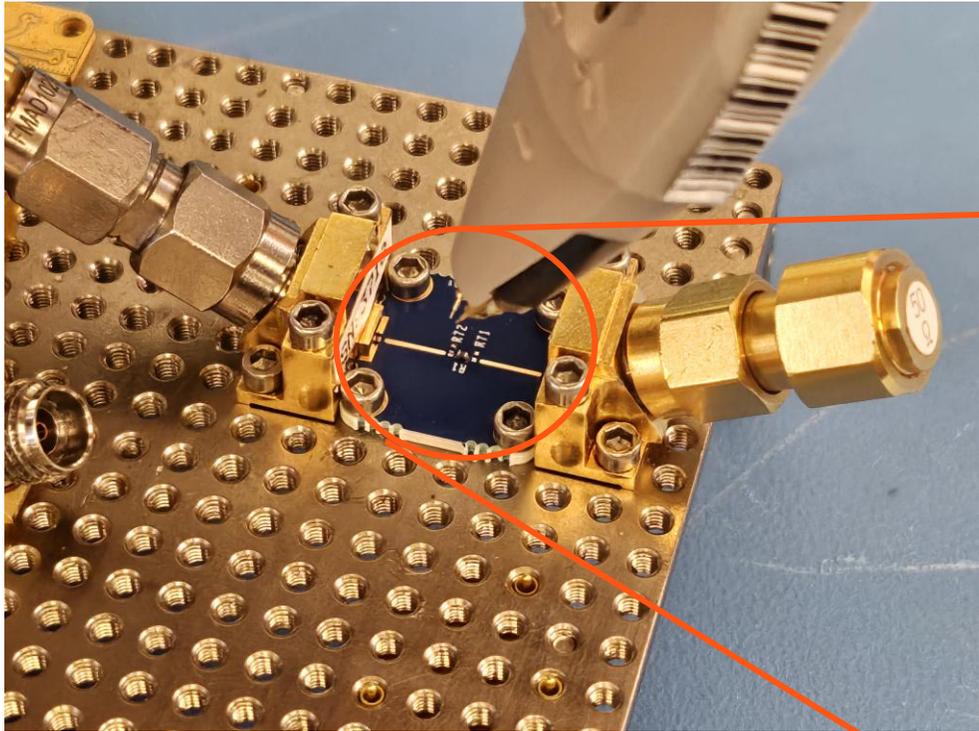
# Evolution From Individual Probes



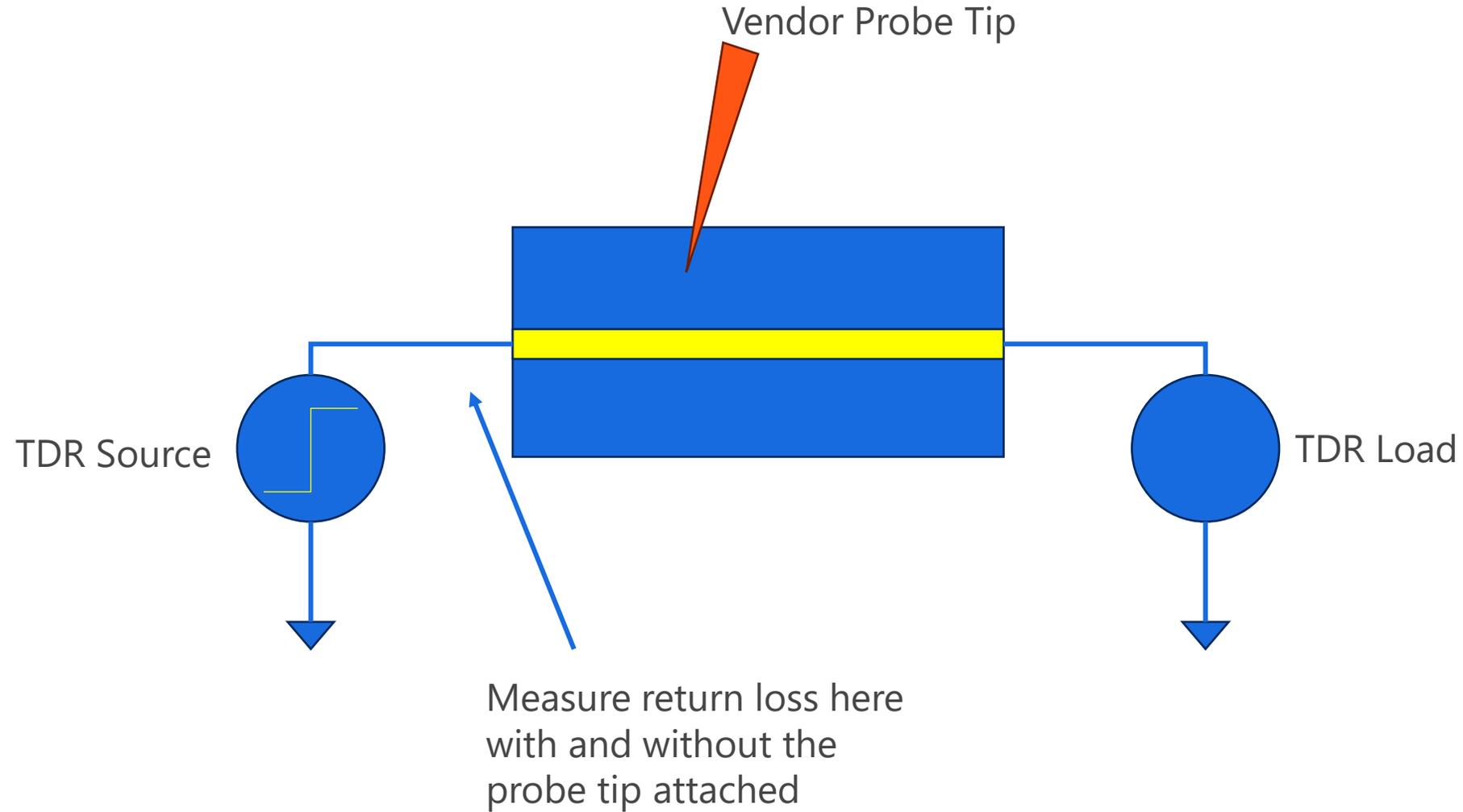


# The Problem With Other Vendor Probes

# Expensive Vendor Probe (1 Channel)



# Too Much Loading (Return Loss Issue)



# Too Much Loading (Return Loss Issue)

NO PROBE



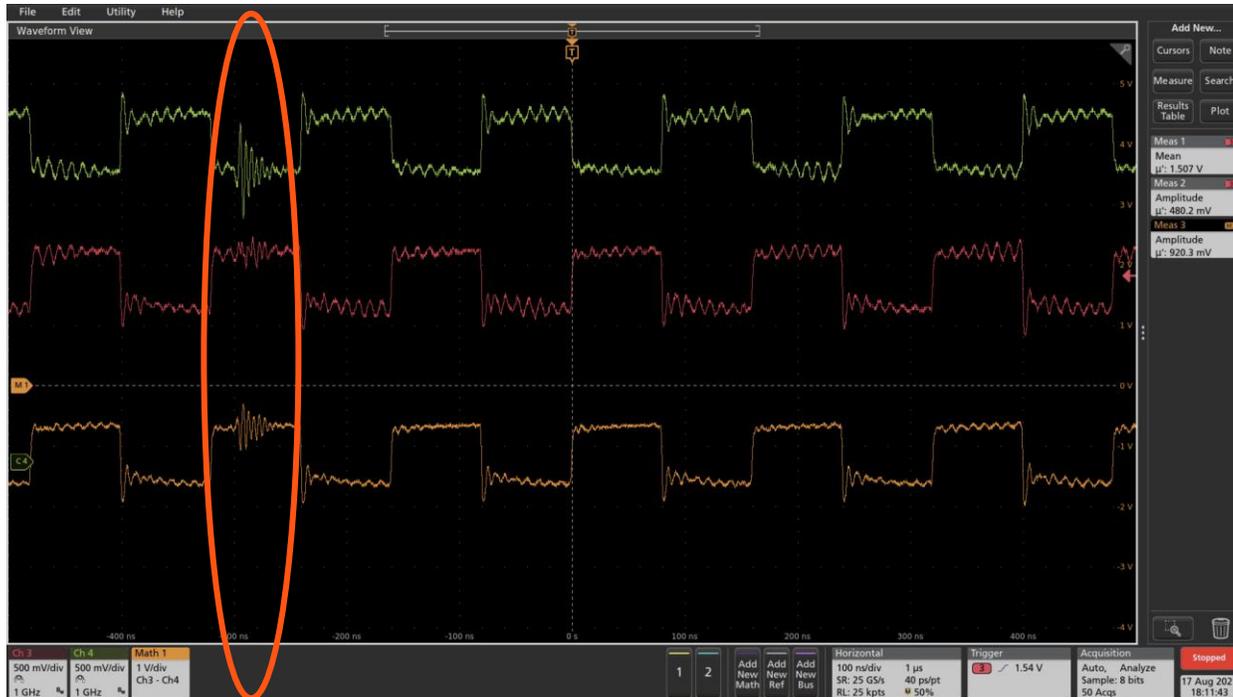
WITH PROBE



44

Introspect's return loss performance is 5x-8x better!

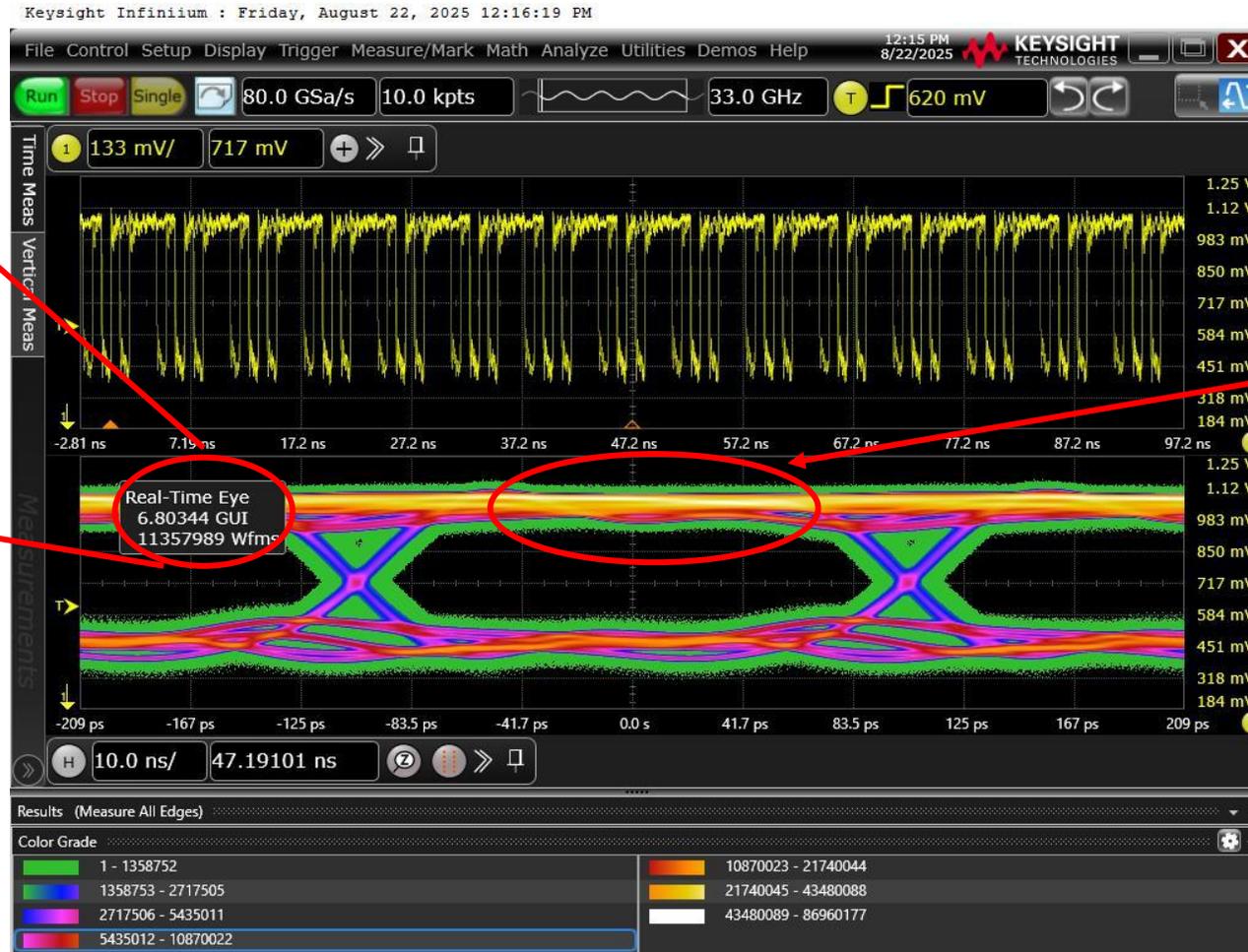
# Too Much Noise



**DDR5 SIGNAL (FROM KEYSIGHT PRESENTATION)**

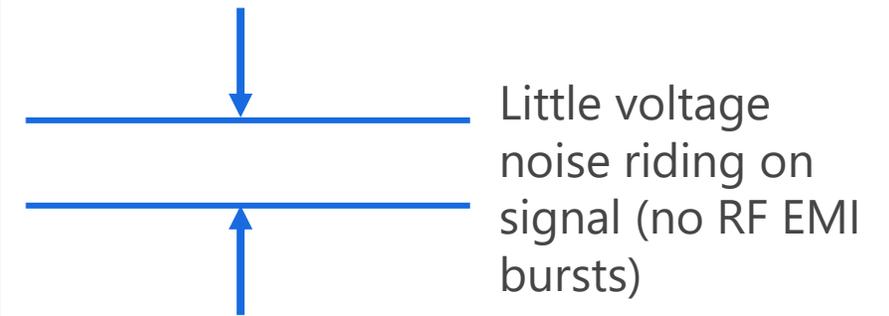
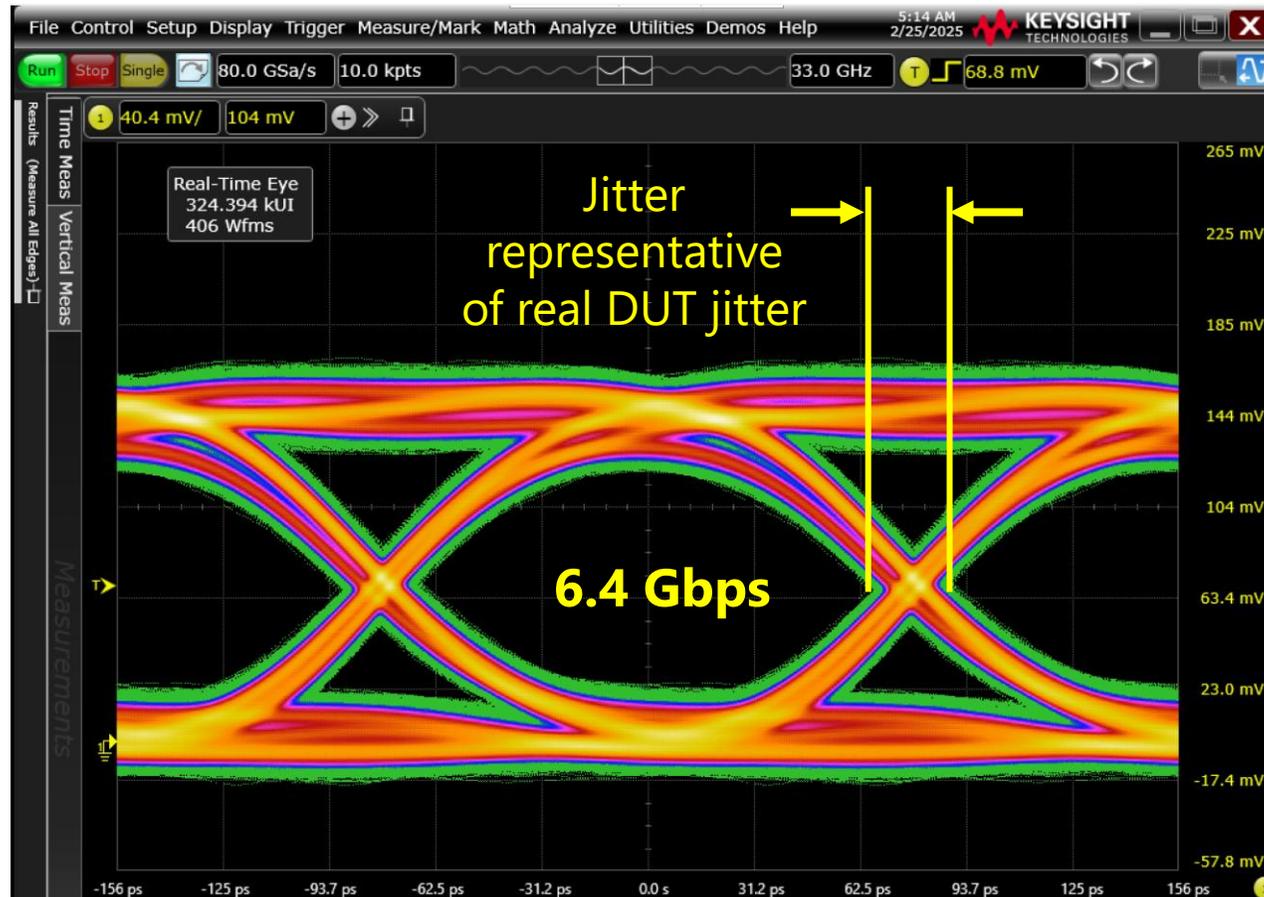
# Introspect's Noise Performance

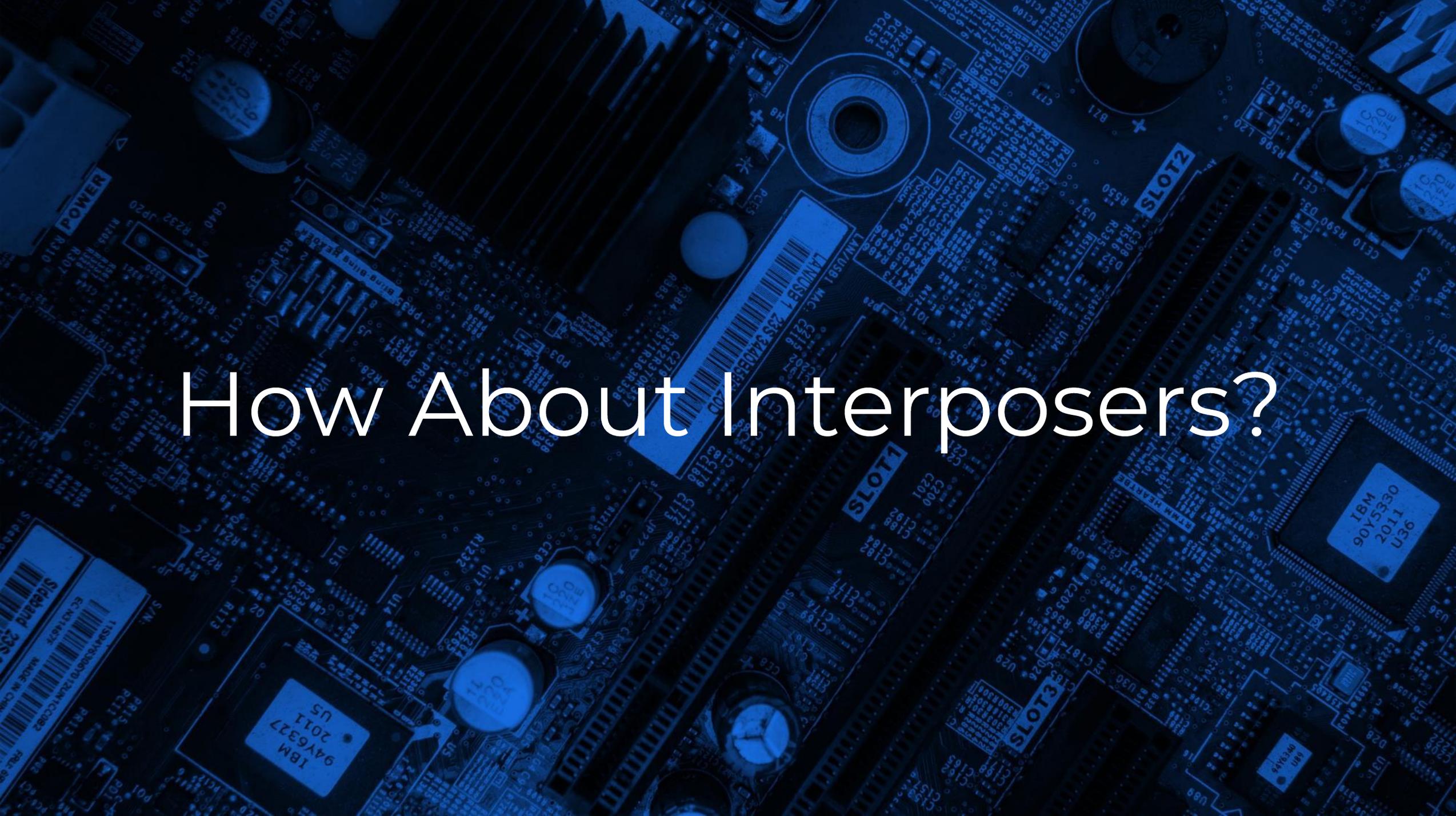
Real-Time Eye  
6.80344 GUI  
11357989 Wfms



No EMI noise effects even after 26 hours of continuous probing

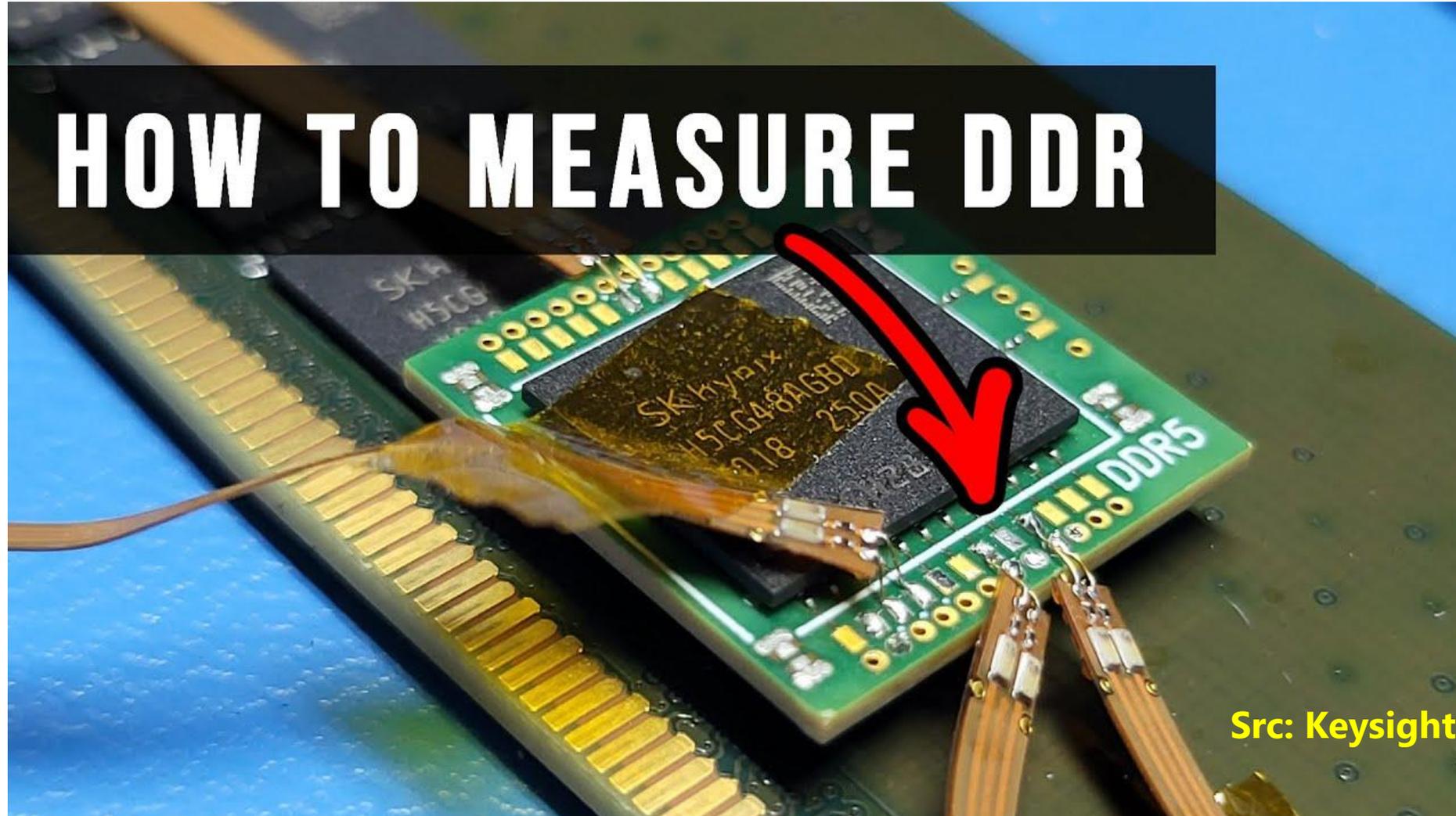
# Another Example (LPDDR5)





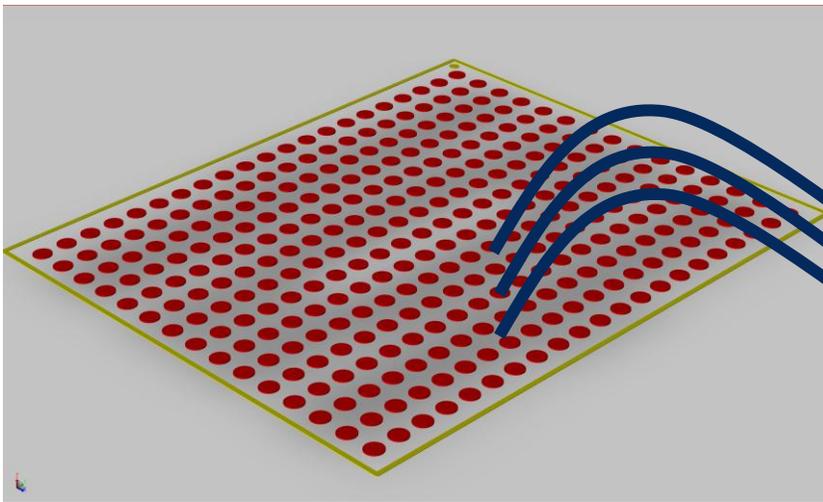
# How About Interposers?

# Standard Packages, But Lots of Channels



# Our Interposer Is Tuned to the RSH!

INTERPOSER

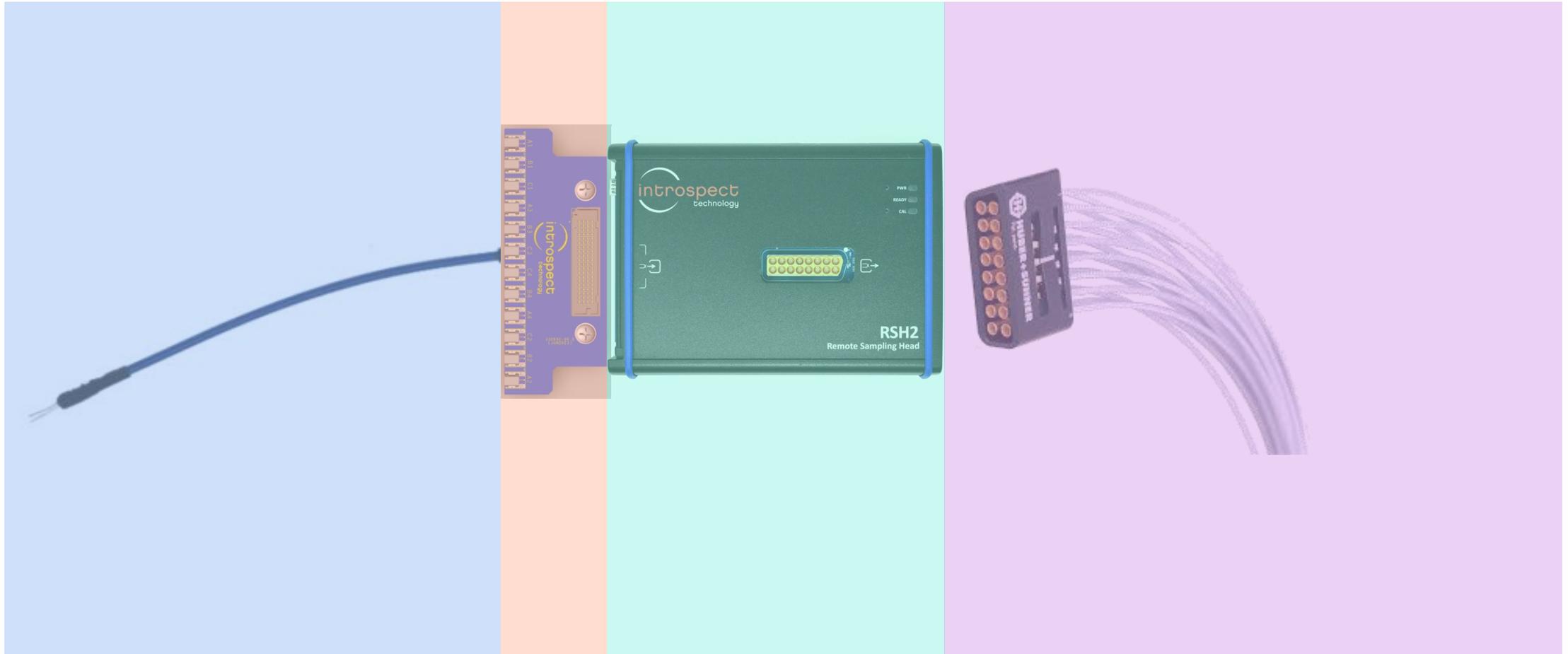


ACTIVE PROBE

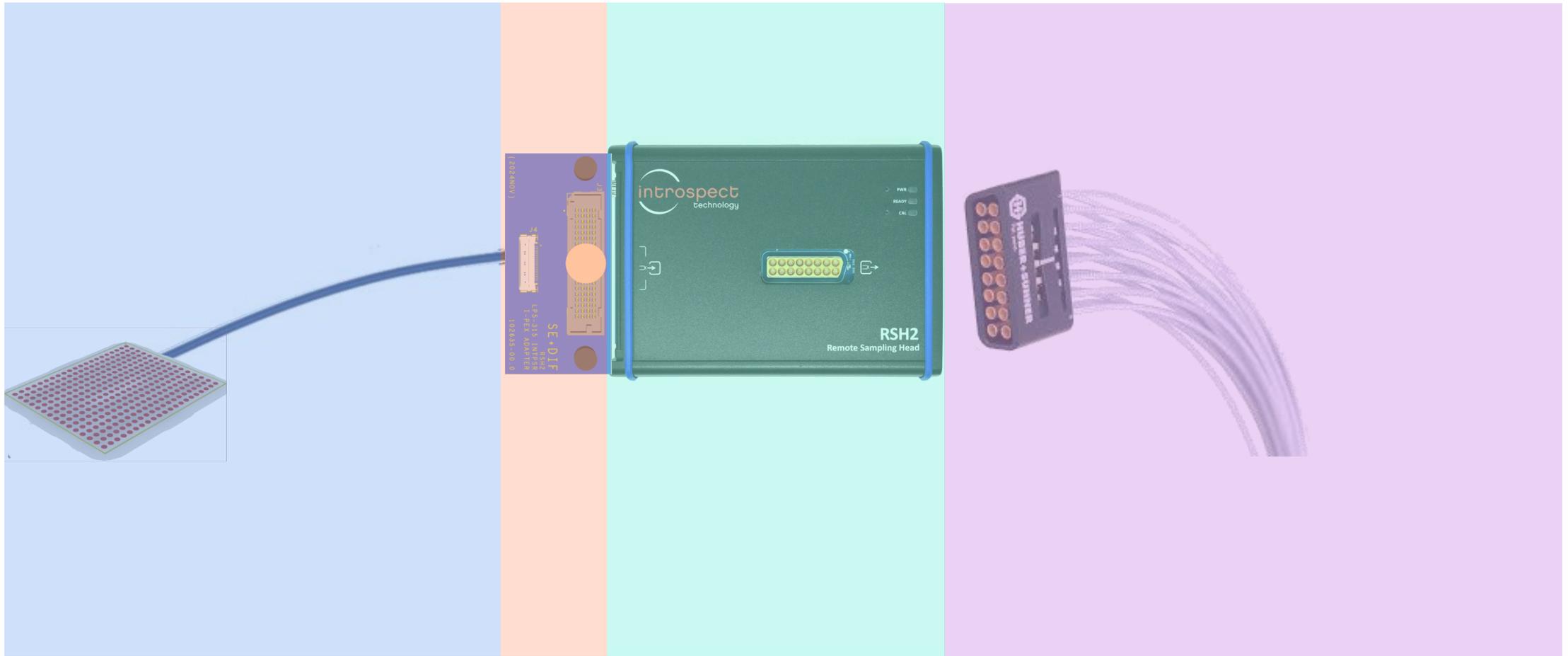


Any 50 Ohm Oscilloscope

# Evolution From General-Purpose RSH



# Evolution From General-Purpose RSH



52

**SOLDER TIP\***

**TIP  
ATTACHMENT**

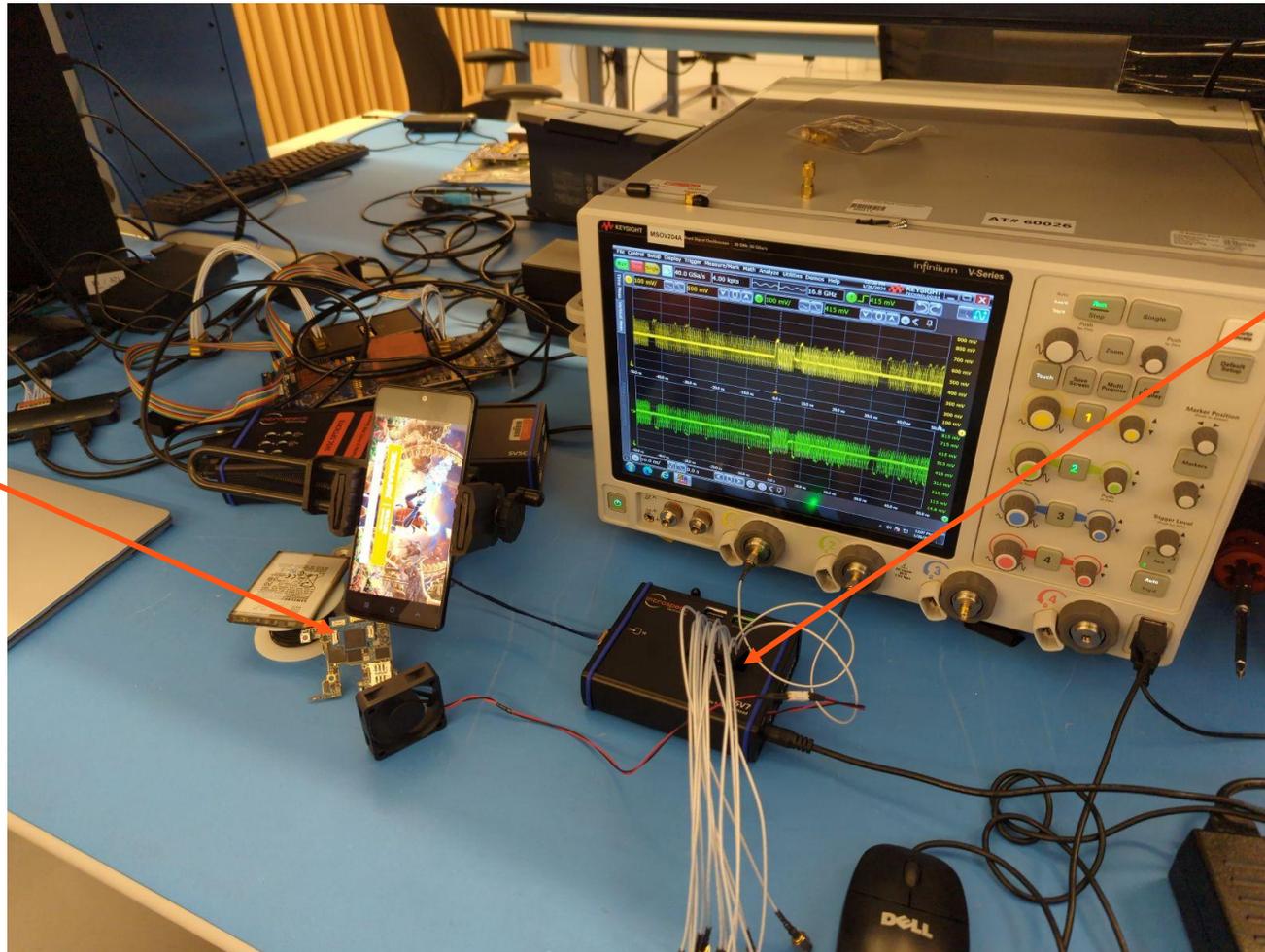
**AMP**

**INSTRUMENT  
ATTACHMENT**



# Real LPDDR5 Example

Interposer system  
(example shown is  
PoP LPDDR5)



Remote Sampling  
Head (multi-channel  
active probe)  
connected to  
oscilloscope

Select different  
channels by  
changing the output  
of the active probe,  
not the soldered  
interposer.

# Interposer Performance

## LIVE LPDDR5X FORMFACTOR PROBING AT 8533 MT/S





## SIGNAL INTEGRITY BENCH



# Interposer Summary

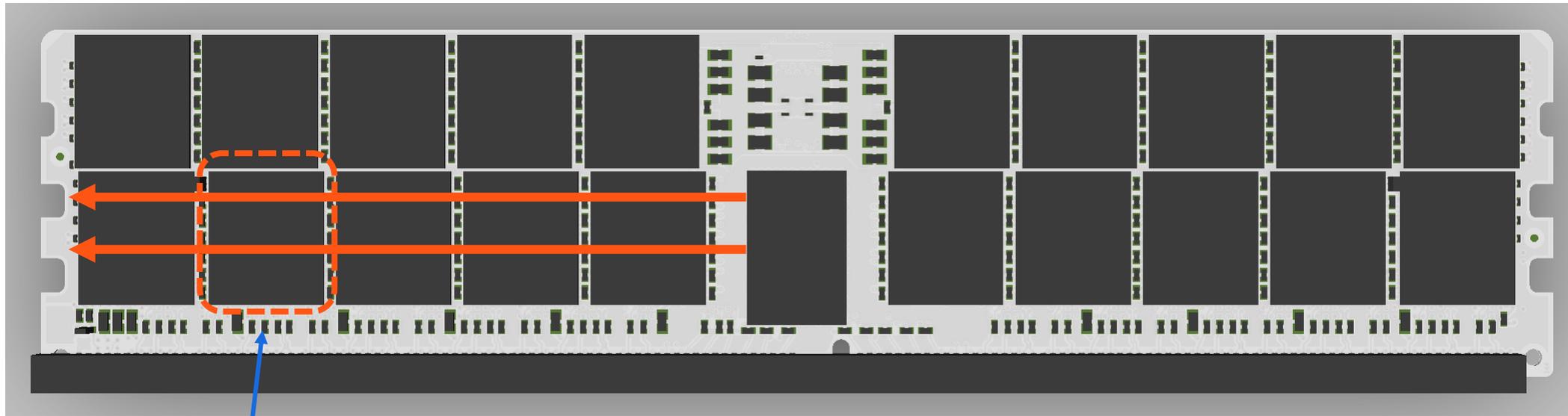
- Introspect's solution is groundbreaking because
  - It can work with **any oscilloscope**
  - It offers **superior performance**



# Where to Probe?

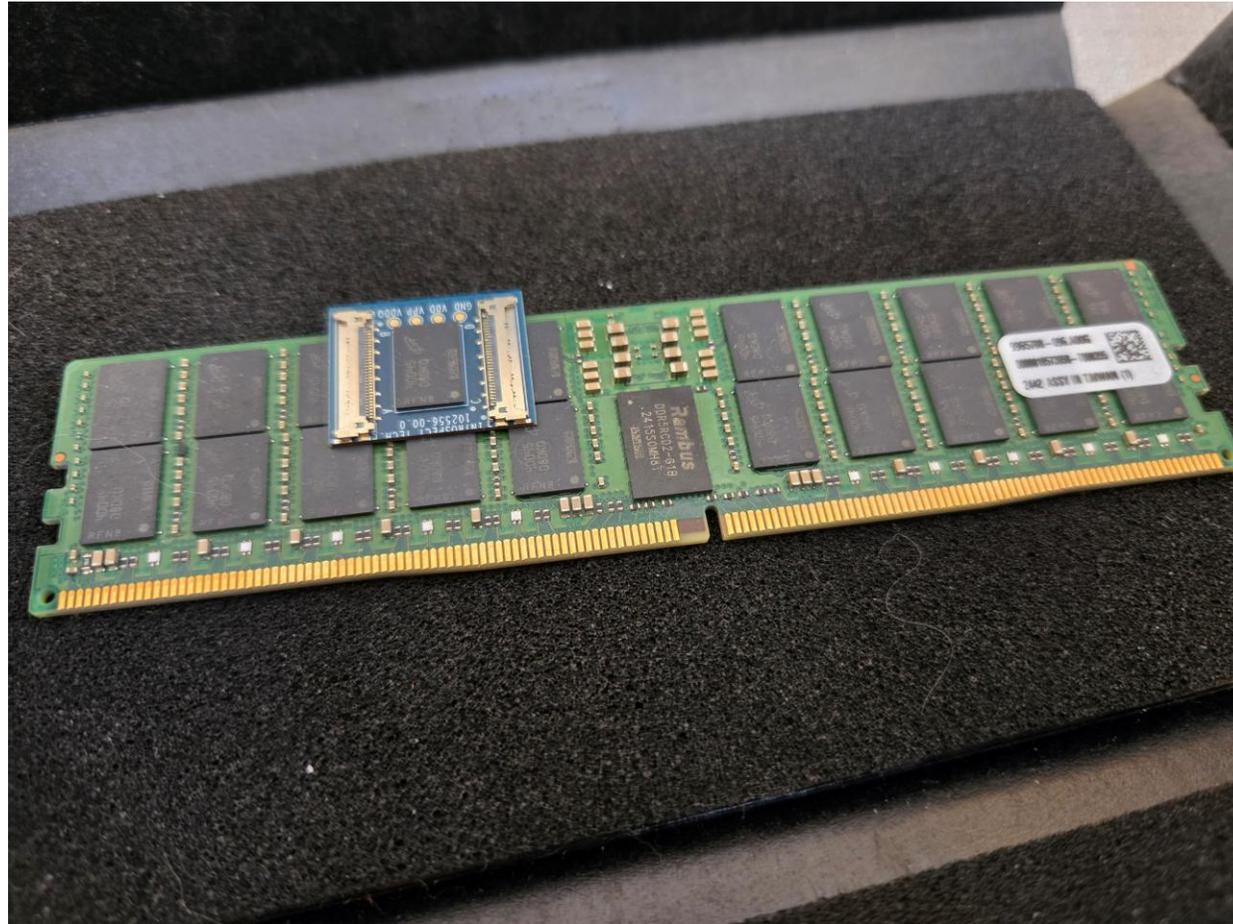
# QCA Bus

## UNIDIRECTIONAL MULTI-DROP BUS FROM RCD TO DRAM



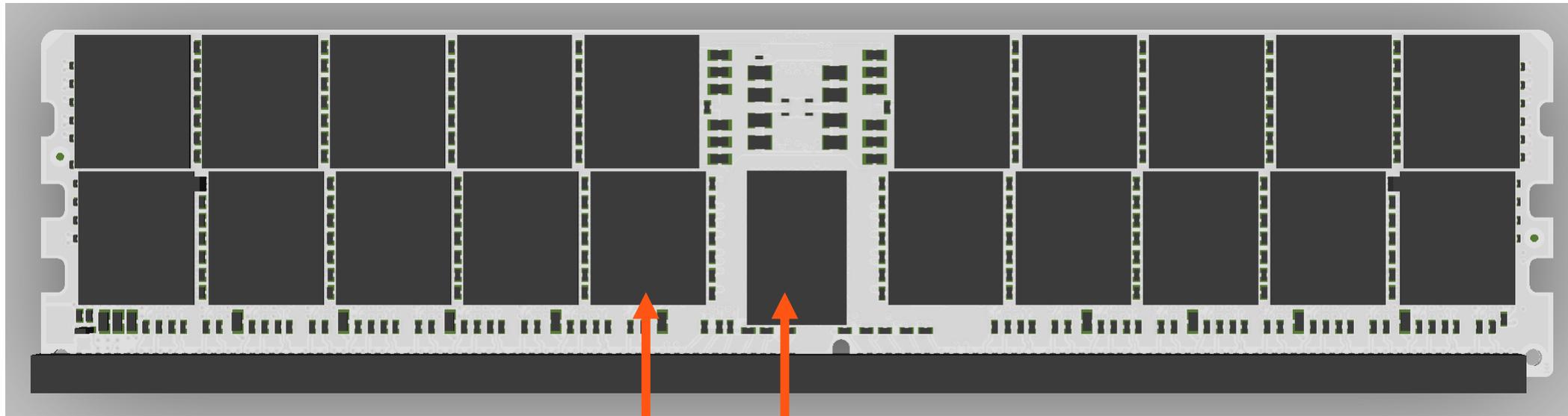
Place integrated-tip interposer under any DRAM

# QCA Bus – Example

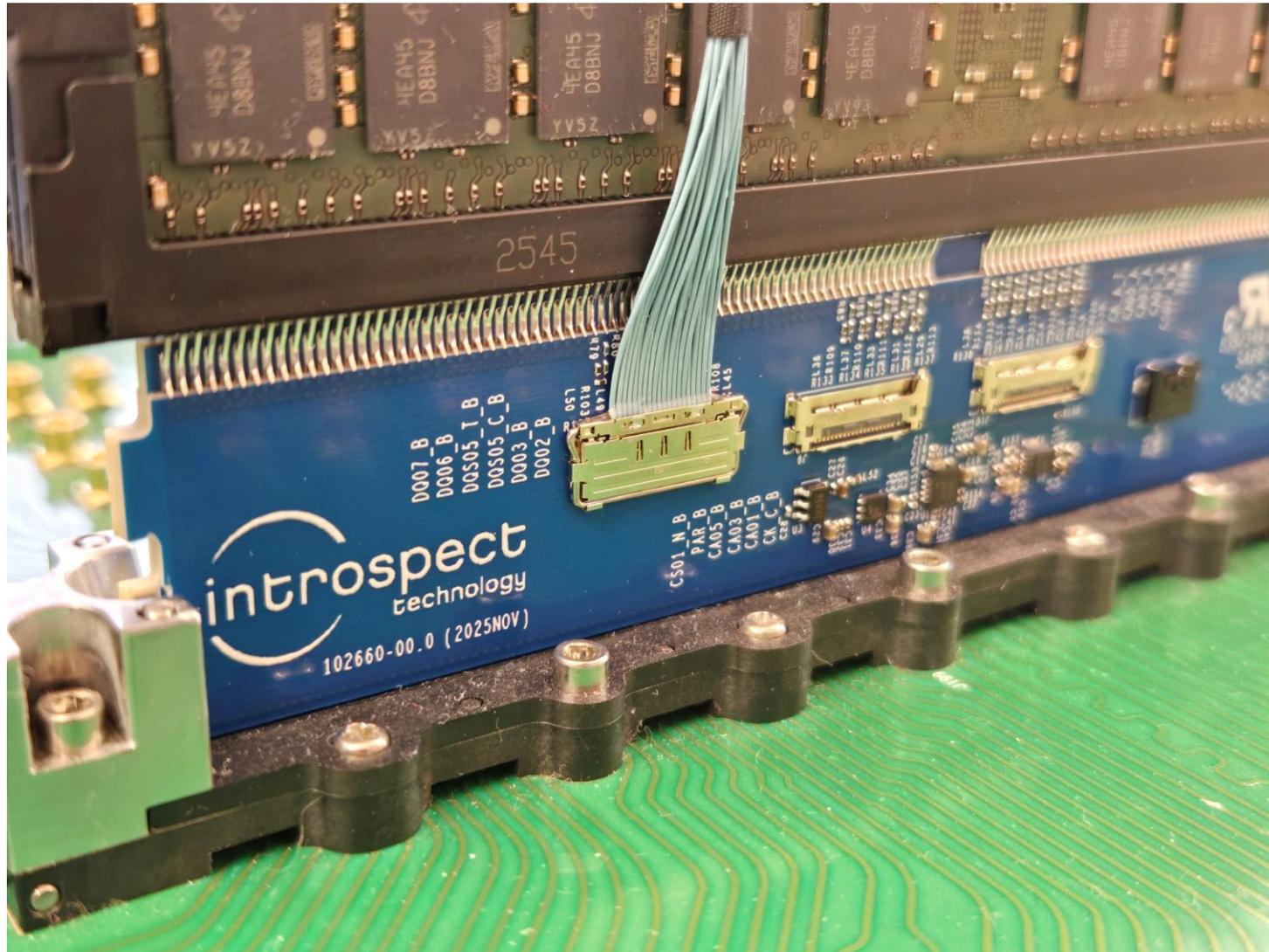


# CA Bus & DQ Write Operations

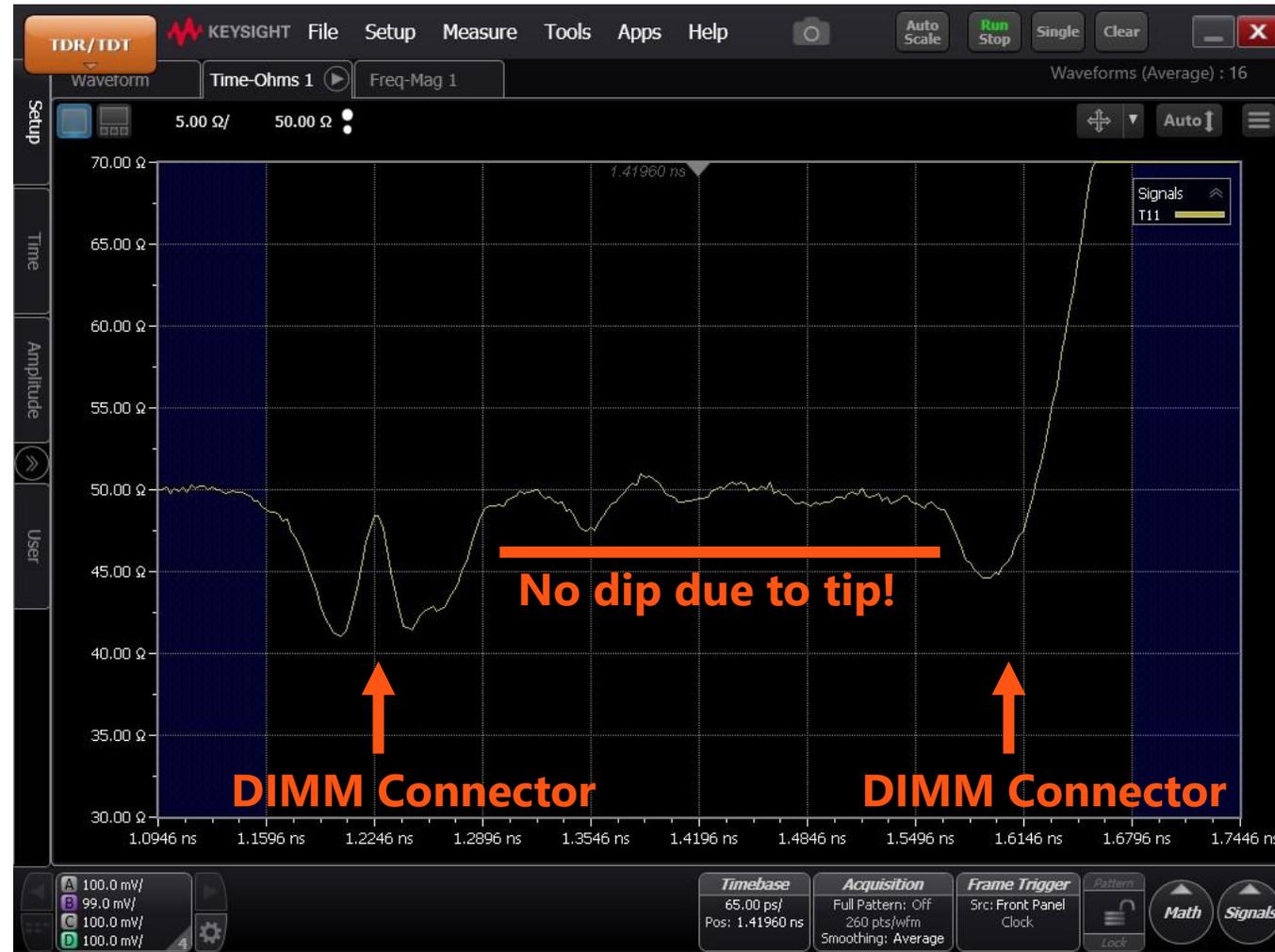
FROM MEMORY CONTROLLER PHY TO DIMM



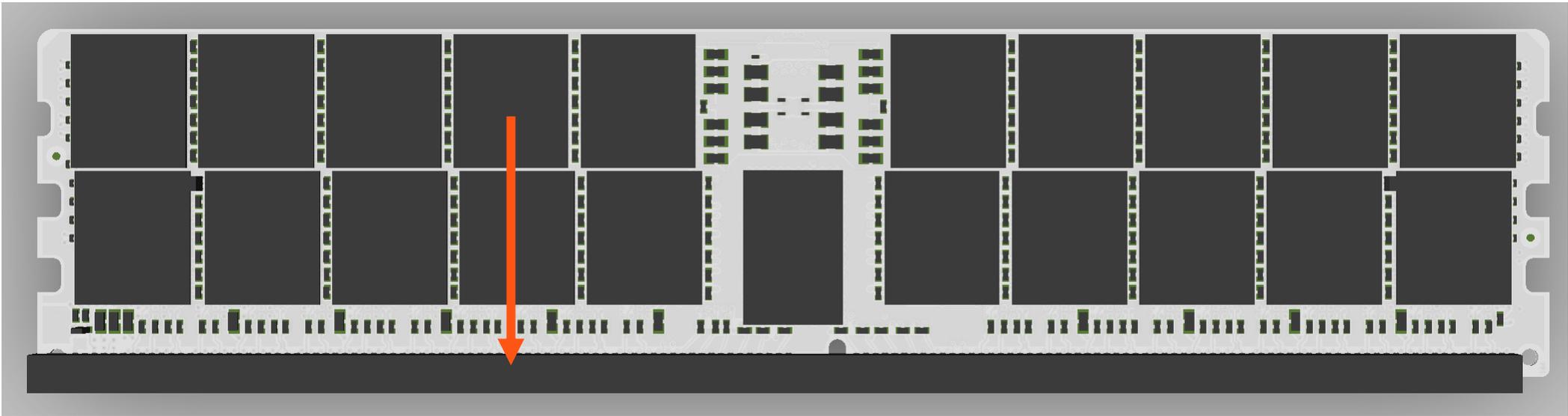
# RDIMM "Riser" Integrated-Tip Interposer



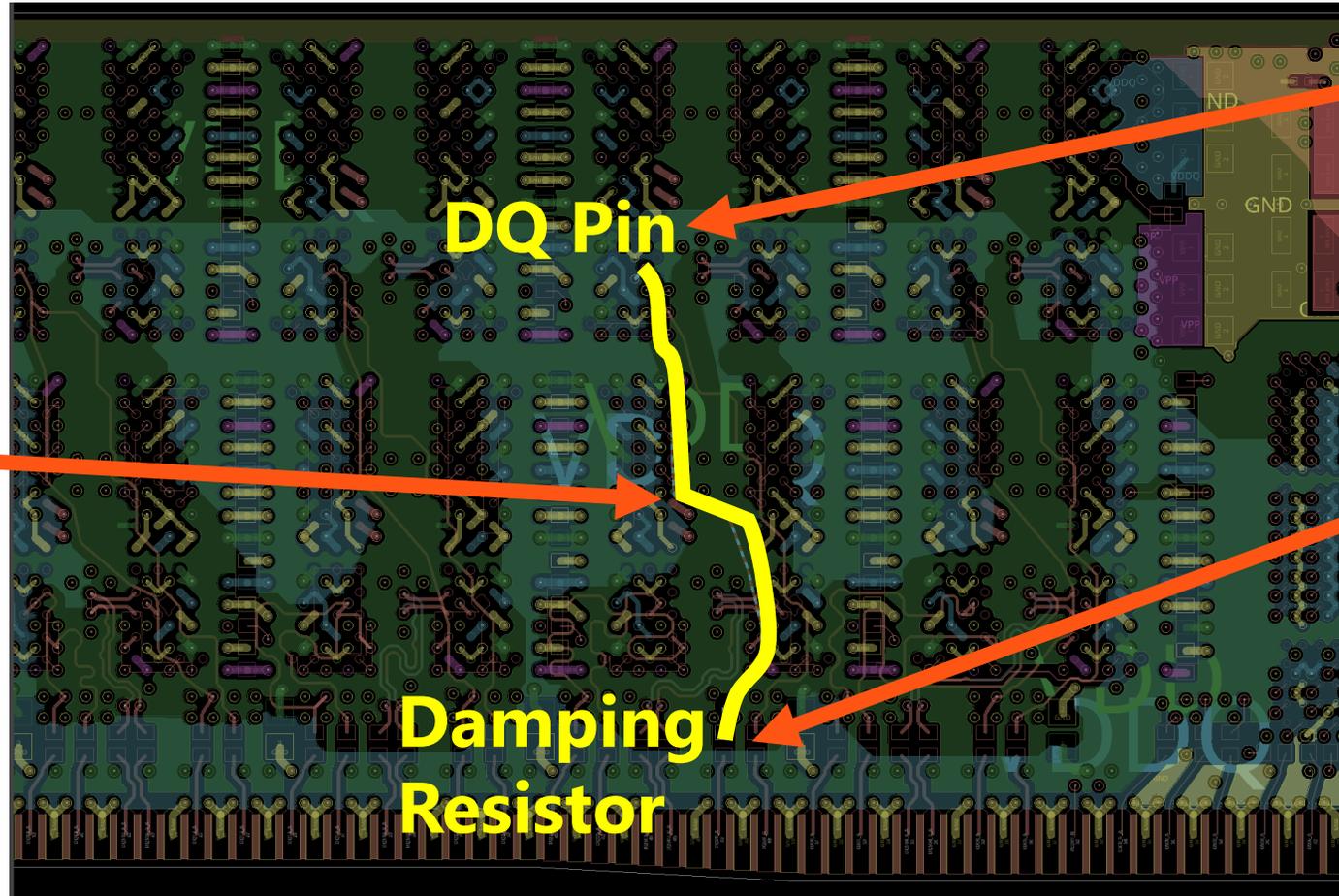
# Interposer Return Loss



# What If You Probe DQ Read at the Source?



# Real DIMM Layout



Long trace acts like a transmission line

Interposer placed under DRAM

This resistor creates reflections!

# Integrated-Tip Interposer Result

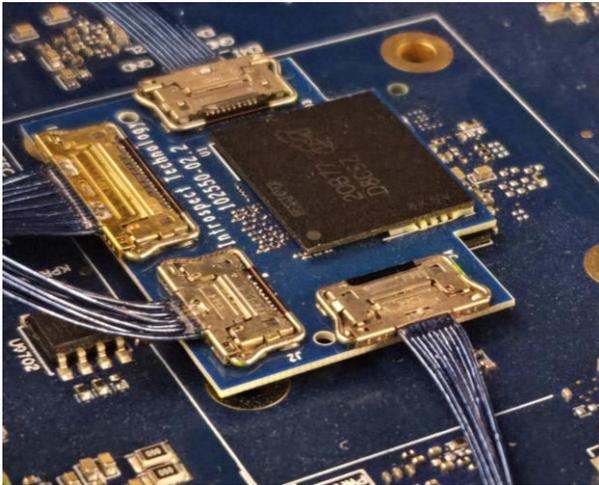


Setup acts as a TDR. Integrated tip interposer still shows extremely low noise.

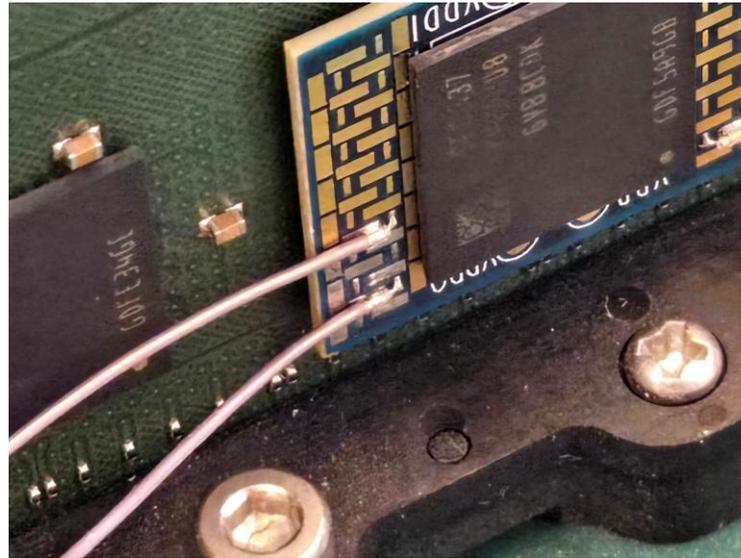
# Integrated-Tip Interposer Portfolio

HELPING YOU OPTIMIZE THE PROBING LOCATION AND USE CASE

Component with I-PEX  
Connectors

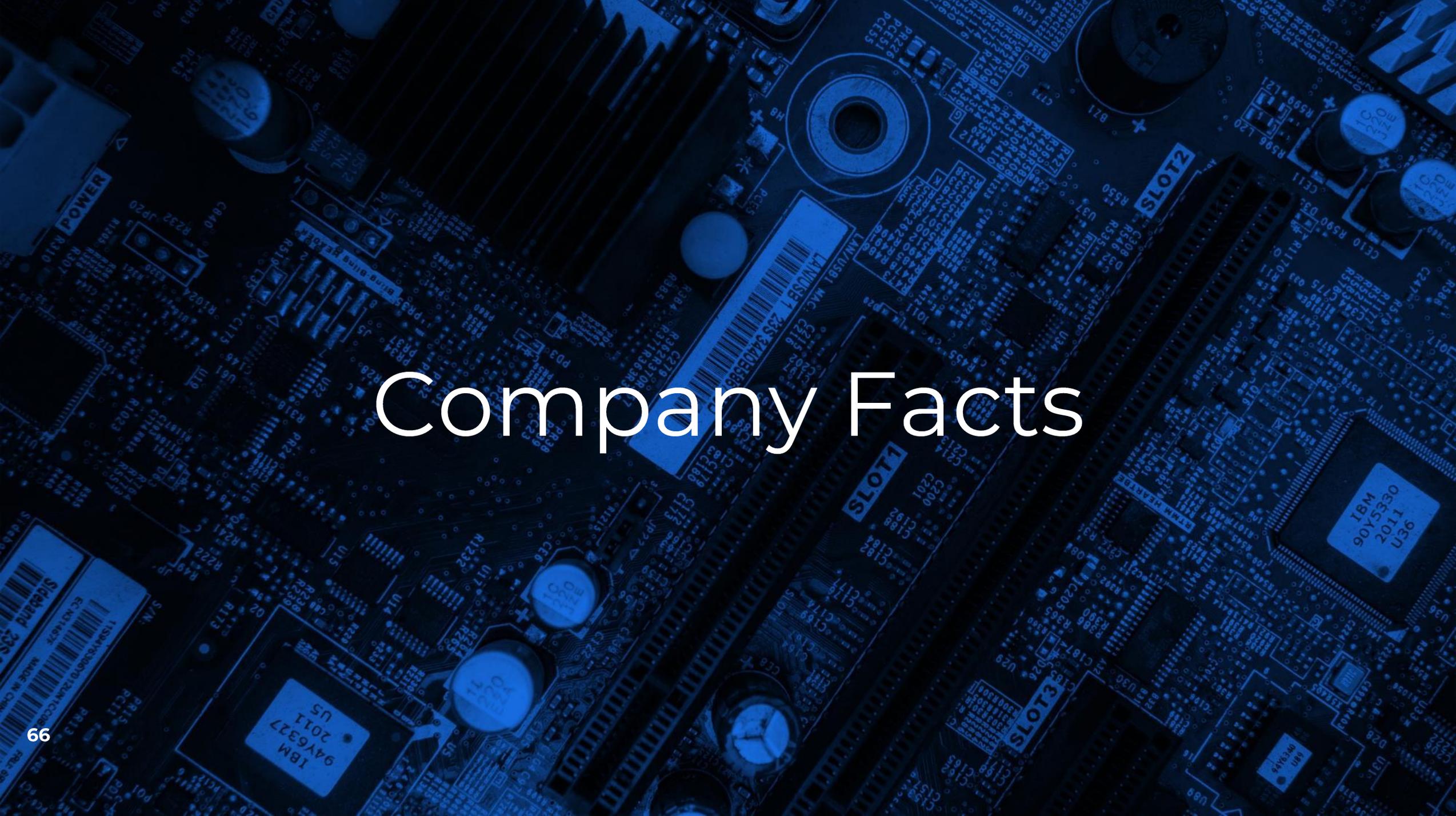


Component with Passive Cables



Module

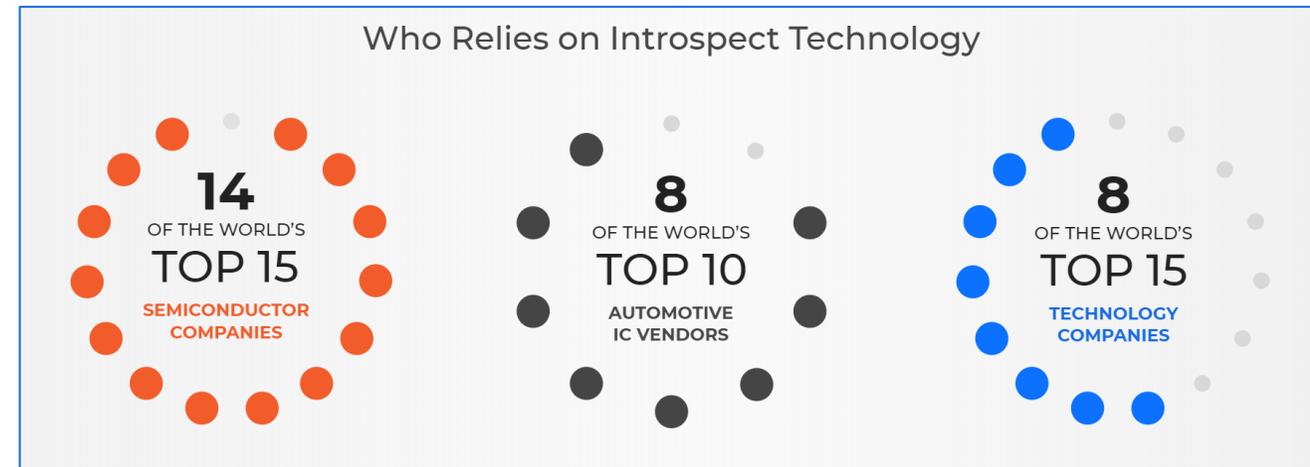




# Company Facts

# Company Facts

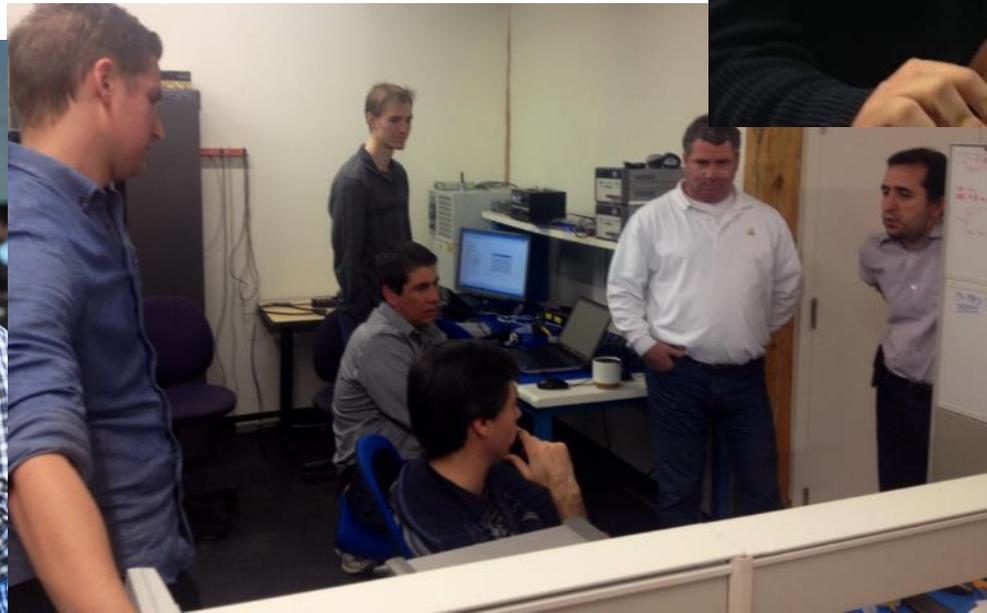
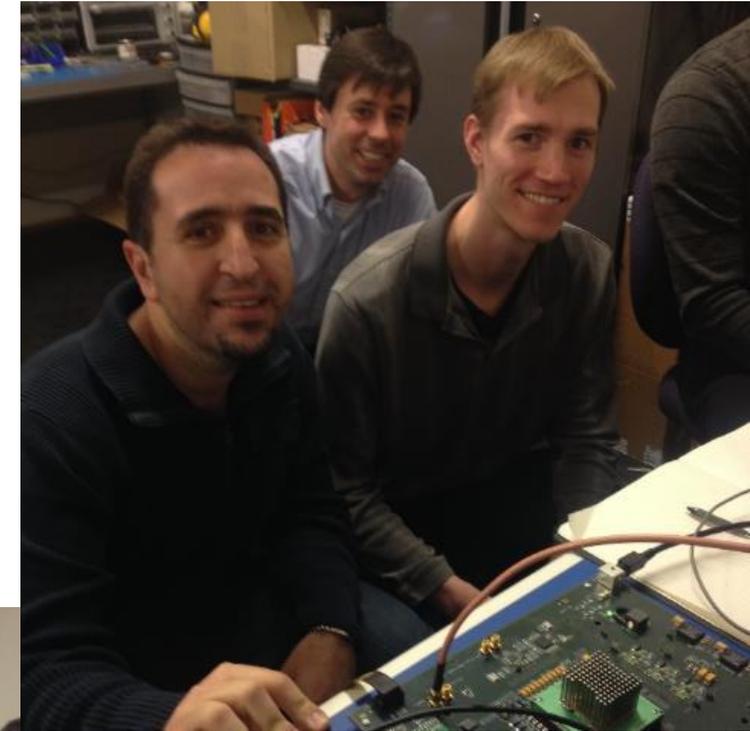
- Founded in **2012**
- Offices in **Montréal, Québec** and **Vancouver, British Columbia**
- **Global, outsourced** sales and distribution channel
- Manufacturer of capital equipment used in the **design validation** and **mass production testing** of electronic components that contain high-speed communications interfaces
  - Smartphones
  - Personal computers and tablets
  - Augmented reality headsets
  - Automotive systems and self-driving systems
  - Data center server racks
  - Medical equipment



# Organizational Performance

## COHESIVE, SKILLFUL DEVELOPMENT TEAM

- Five generations of products and growing
- Core competence in microwave design, hardware design, software design, and algorithm design
- Worldwide support coverage
- Team behind the **world's first** MIPI C-PHY solutions among many other firsts



# Organizational Performance

## RECOGNIZED INDUSTRY LEADERSHIP

- Contributor member at [MIPI Alliance](#), [JEDEC](#), [PCI-SIG](#), [Vesa](#), others
- Electronics Industry Awards Test & Measurement Product of the Year (2024) for the [M5512 GDDR7 Memory Test System](#)
- Future of Memory & Storage (FMS) Best of Show (2024)
- Electronics Industry Awards [Excellence in Innovation](#) (2022) and [Best Customer Service](#) (2021)
- Electronics Industry Awards, [T&M and EDA tools](#), 2019, 2020, 2021
- Best in Design & Test Award 2013, 2015 (based on user votes)
- Finalist for ACE [Executive of the Year](#) Award 2014
- Finalist for ACE [Design Team of the Year](#) Award 2015



EXCELLENCE IN INNOVATION



# Deployment Areas

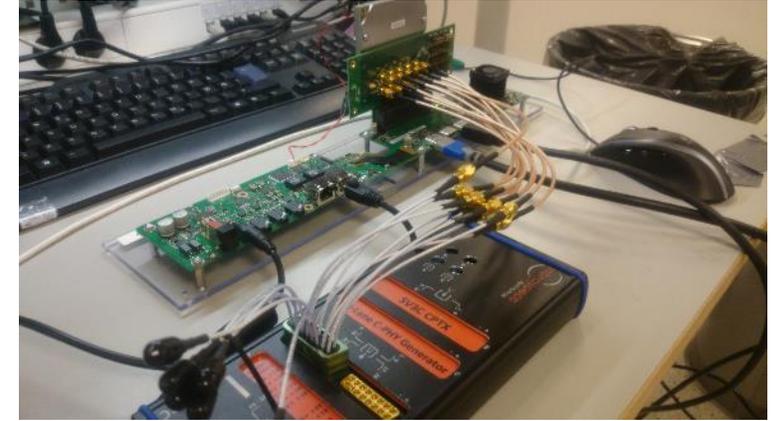
**Electrical Characterization**



**Design Validation**



**Applications Engineering**



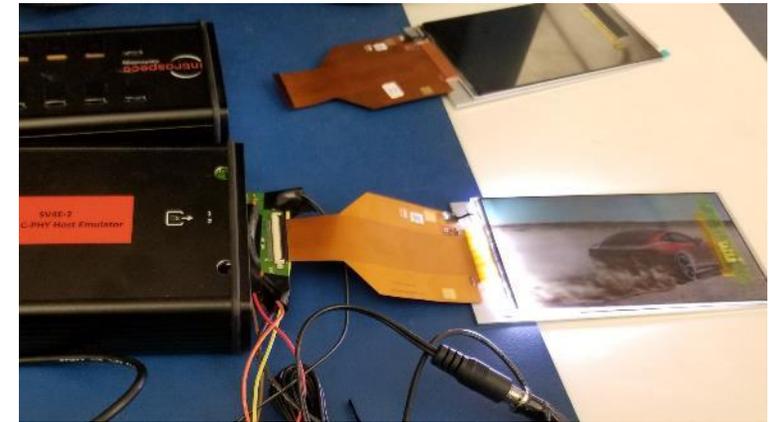
**Production Testing**



**Failure Analysis**



**System-Level Test**



# Summary

## HIGHLY DIFFERENTIATED SOLUTIONS

- Introspect develops **parallel** test instruments for high-speed interfaces
- Our solutions **fill a much-needed gap** in test and measurement equipment availability
- We have created a rich portfolio of solutions for MIPI, DisplayPort, memory interfaces, and others
- Our solutions can be deployed at the **component level** and at the **module level**