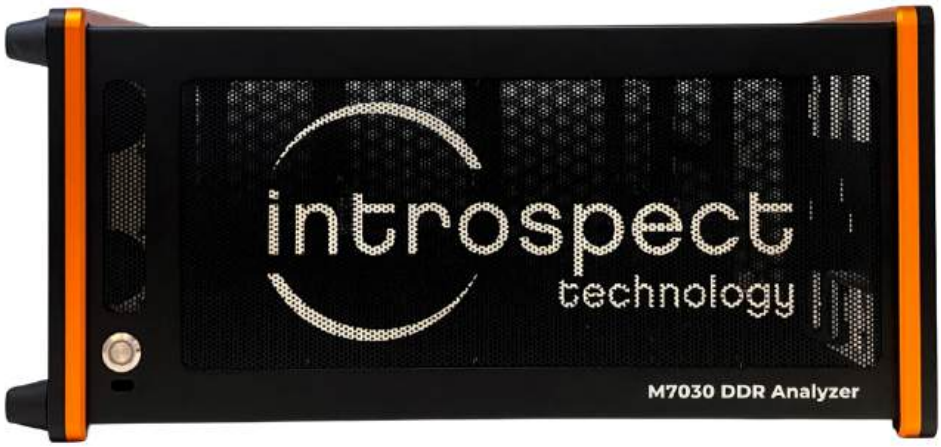
DATA SHEET

M7030 DDR/LPDDR Protocol Analyzer

M SERIES



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INTROSPECT.CA

Table of Contents

Introduction

OVERVIEW

The M7030 DDR/LPDDR Protocol Analyzer is a high-sampling-rate logic and protocol analysis solution for advanced memory debug, validation, and compliance testing. With sampling rates up to 80 GS/s, support for DUT transfer rates up to 20,000 MT/s, and visibility into up to 36 command/address and data signals, the M7030 Analyzer captures complete read/write activity across a full memory channel. High-impedance active probing and dedicated integrated-tip interposers provide deep protocol and electrical insight into DDR, LPDDR, HBM, and GDDR systems without disturbing live memory operation.

KEY FEATURES

- High-speed logic and protocol analysis with sampling rates up to 80 GS/s.
- DUT transfer-rate support up to 20,000 MT/s.
- Complete command/address and data capture across up to 36 single-ended receiver channels.
- High-level protocol decoding that converts DDR/LPDDR logic waveforms into human-readable commands.
- Timing parameter measurements with automatic, specification-based violation flagging.
- Clock-aware capture that tracks clock frequency changes and continues seamlessly through clock-stop events.
- Command-based capture triggers.
- DDR/LPDDR truth-table commands such as ACT1, CAS, MPC, and custom commands.
- Training-free operation using live voltage and phase compensation.
- 24 Gbytes of on-board memory with advanced filtering for long trace captures.
- Active probing and dedicated integrated-tip interposers for high-bandwidth measurement with simplified de-embedding.

KEY BENEFITS

- Debug memory systems faster by turning complex DDR/LPDDR waveforms into readable command and timing views.
- Validate live memory traffic without disturbing communication between the controller and memory device.
- Capture complete read/write transactions by observing command/address and data activity in parallel.

- Analyze dynamic memory behavior through clock changes, clock stops, and low-power transitions.
- Support longer debug scenarios with deep on-board memory and advanced filtering.
- Correlate electrical and protocol behavior using the same interposers and RSH active-probe technology.
- Scale analysis across DDR, LPDDR, HBM, and GDDR applications.
- Improve signal integrity during probing through high-impedance active probes, shielded cables, and dedicated interposers.
- Reduce setup complexity with integrated-tip interposer options and interchangeable RSH adapters.

ANALYZER CONCEPT

DDR/LPDDR Link *Sniffer*

The M7030 Analyzer provides non-intrusive visibility into live memory traffic by operating as a link sniffer between the memory controller and the DRAM device. Because the analyzer is neither a source nor a sink, the controller and memory continue normal communication while the analyzer observes and captures protocol activity.

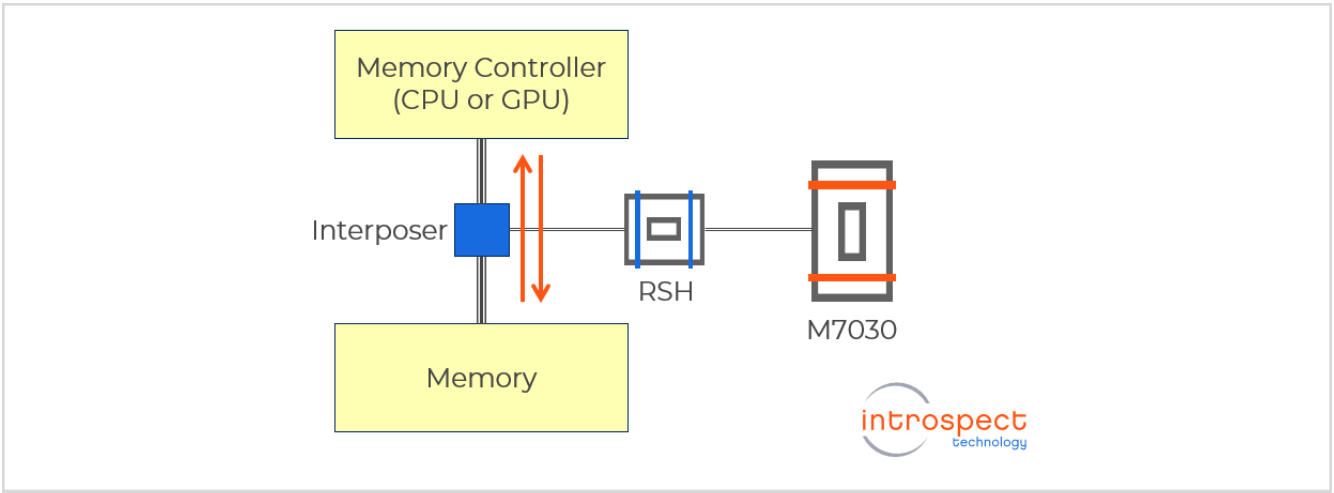


Figure 1: Connection Diagram

Feature Description

CAPTURE DDR/LPDDR SIGNALS

Aligned Parallel Capture

The M7030 Analyzer captures aligned logic signals across command and data channels, supporting up to 36 independent channels. This parallel capture capability gives engineers a coherent view of DDR/LPDDR bus activity and provides the foundation for accurate protocol decoding and timing analysis.

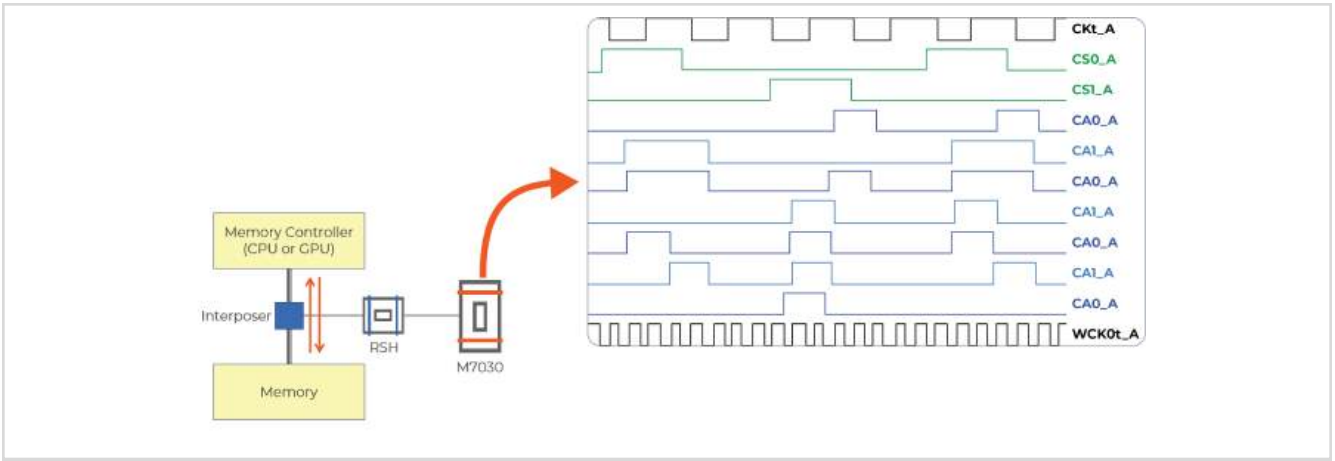
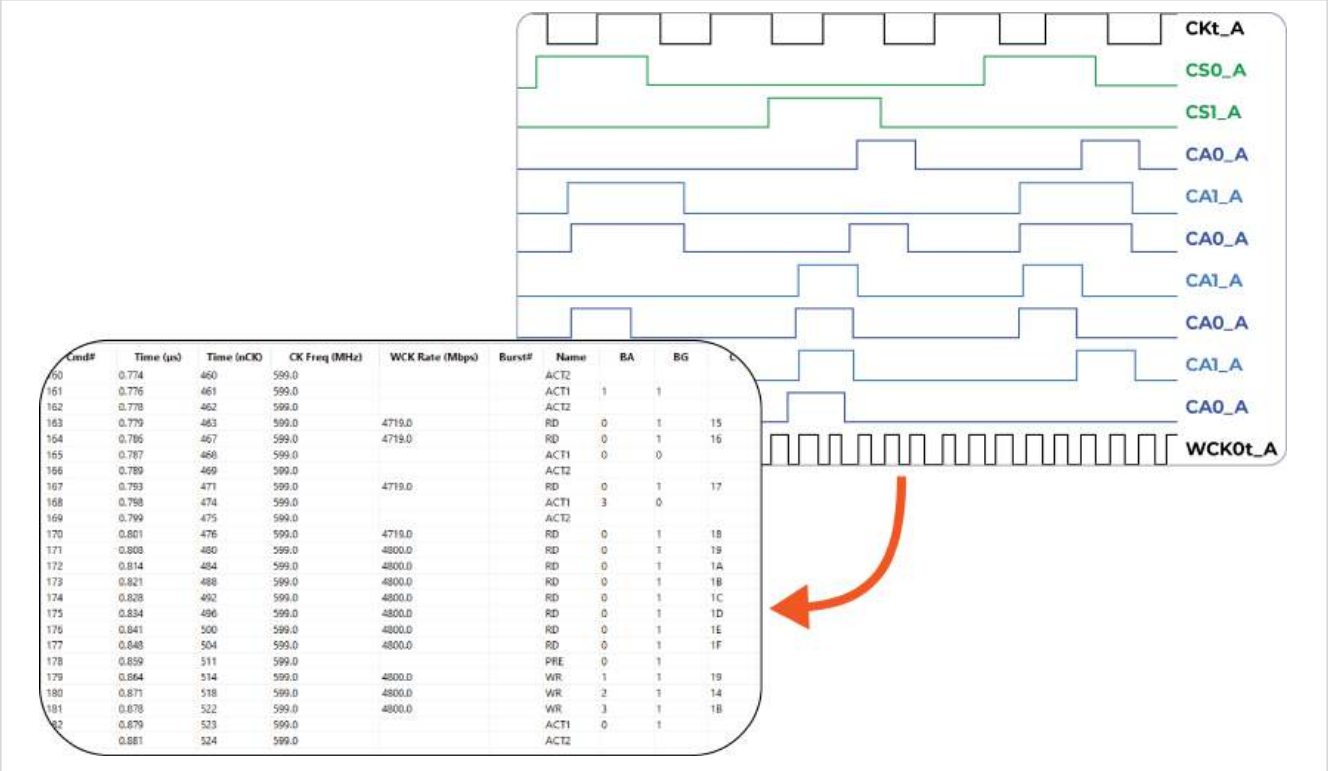


Figure 2: Captured Logic Signals of an LPDDR5 Command Bus

HIGH LEVEL ANALYSIS

Command Decoding

Captured logic signals are automatically interpreted into DDR/LPDDR commands, allowing engineers to move from raw bus activity to meaningful protocol-level information. Decoded command views simplify debug, reduce manual interpretation, and accelerate root-cause analysis.



Cmd#	Time (µs)	Time (nCK)	CK Freq (MHz)	WCK Rate (Mbps)	Burst#	Name	BA	BG	C
160	0.774	460	599.0			ACT2			
161	0.776	461	599.0			ACT1	1	1	
162	0.778	462	599.0			ACT2			
163	0.779	463	599.0	4719.0		RD	0	1	15
164	0.786	467	599.0	4719.0		RD	0	1	16
165	0.787	468	599.0			ACT1	0	0	
166	0.789	469	599.0			ACT2			
167	0.793	471	599.0	4719.0		RD	0	1	17
168	0.798	474	599.0			ACT1	3	0	
169	0.799	475	599.0			ACT2			
170	0.801	476	599.0	4719.0		RD	0	1	18
171	0.808	480	599.0	4800.0		RD	0	1	19
172	0.814	484	599.0	4800.0		RD	0	1	1A
173	0.821	488	599.0	4800.0		RD	0	1	1B
174	0.828	492	599.0	4800.0		RD	0	1	1C
175	0.834	496	599.0	4800.0		RD	0	1	1D
176	0.841	500	599.0	4800.0		RD	0	1	1E
177	0.848	504	599.0	4800.0		RD	0	1	1F
178	0.859	511	599.0			PRE	0	1	
179	0.864	514	599.0	4800.0		WR	1	1	19
180	0.871	518	599.0	4800.0		WR	2	1	14
181	0.878	522	599.0	4800.0		WR	3	1	1B
182	0.879	523	599.0			ACT1	0	1	
	0.881	524	599.0			ACT2			

Figure 3: Logic Signals to LPDDR Commands

Captured Trace Organization

Using Pinetree™, the protocol analyzer viewer presents decoded DDR/LPDDR commands in a structured, navigable interface. Engineers can review captured bus activity at a higher level of abstraction, making it easier to identify command flow, transactions, and areas requiring closer inspection.

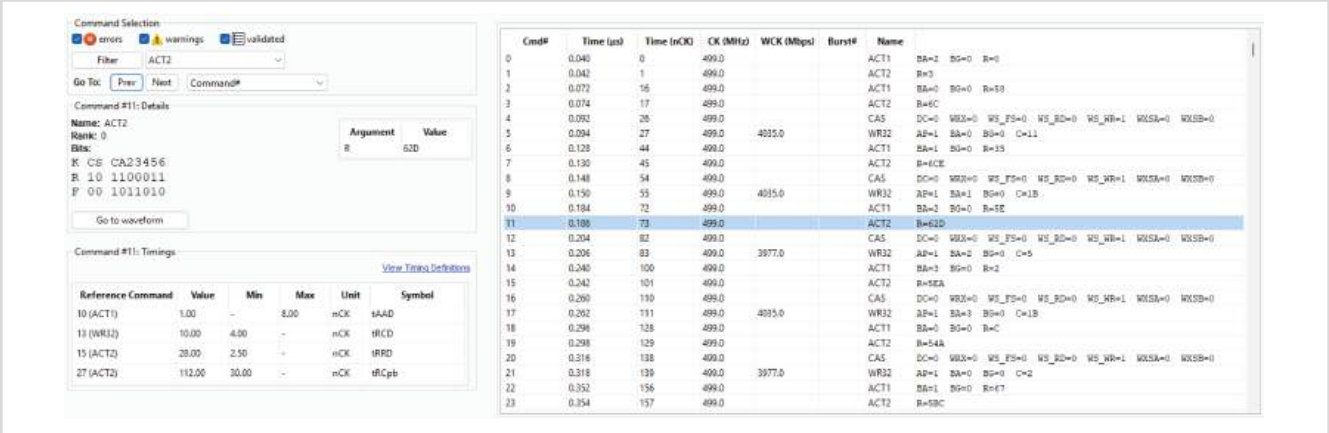
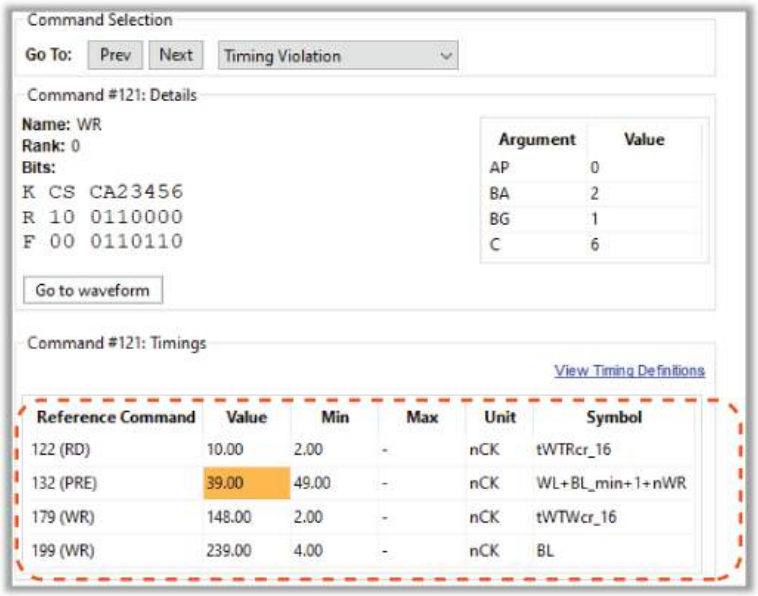


Figure 4: Protocol Analyzer Viewer

Command Timing Analysis

The M7030 Analyzer computes and validates command-specific timing parameters against protocol requirements. Timings that violate the specifications can be quickly identified through search and highlighting, helping engineers isolate subtle issues such as insufficient command spacing or incorrect timing relationships.



Measured timings for a write command are shown above. The timing relative to the "PRE" command is slightly too short, according to the LPDDR specification.

Figure 5: Measured Timings

Command Sequence Validation

In addition to timing checks, the M7030 Analyzer can validate command sequencing to help confirm correct DDR/LPDDR protocol behavior. This capability supports faster verification of memory-controller operation and helps identify protocol-level errors that may be difficult to detect from waveforms alone.

Mode Register Decoding

Mode register transmissions are decoded into readable fields for easier review. Register-specific decoding allows engineers to inspect configuration values directly without having to cross-check with the original JEDEC specifications, reducing the effort required to interpret opcodes and mode register contents manually.

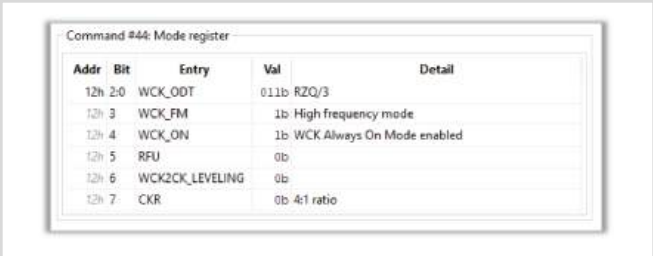
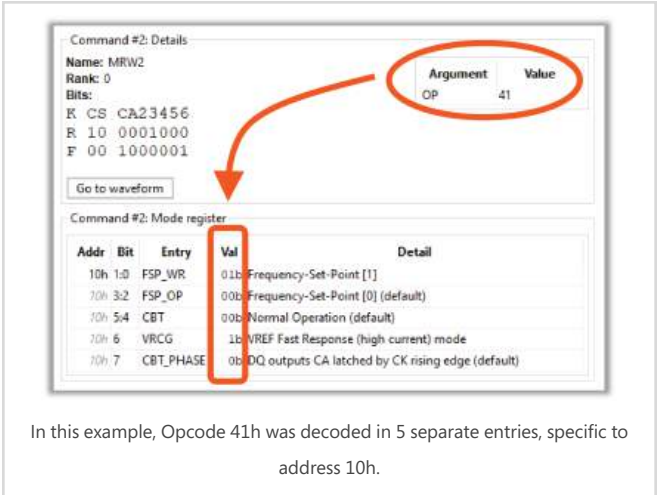


Figure 6: Decoding of Mode Register 12h



In this example, Opcode 41h was decoded in 5 separate entries, specific to address 10h.

Figure 7: Decoding of Mode Register 10h

CLOCK FLEXIBILITY

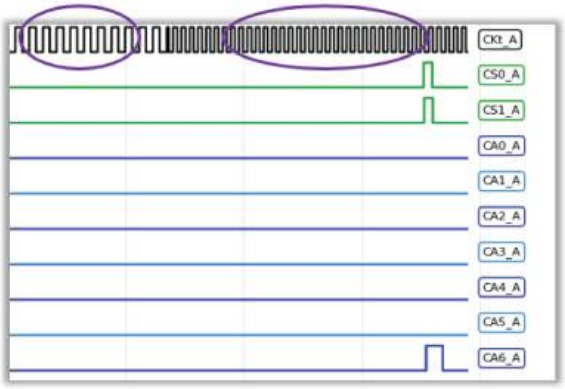
Clock Frequency Change Handling

The M7030 Analyzer is designed to handle rapid clock frequency changes without relying on synchronization to a controller-provided clock. Instantaneous frequency changes are tracked and reflected in the command and signal views, enabling reliable analysis across dynamic memory operating modes.

Cmd#	Time (µs)	Time (nCK)	CK Freq (MHz)	WCK Rate (MI
85	1725.286	517566	300.0	
86	1725.304	517571	300.0	
87	2668.495	800528	300.0	
88	2668.498	800529	300.0	
89	13420.086	0	498.0	
90	15625.041	1104560	498.0	
91	15625.043	1104561	498.0	
92	15797.542	1190356	498.0	

Note that in this example, it resets the timestamp expressed as **nCK**.

Figure 8: Clock Changes Shown in Commands Tab

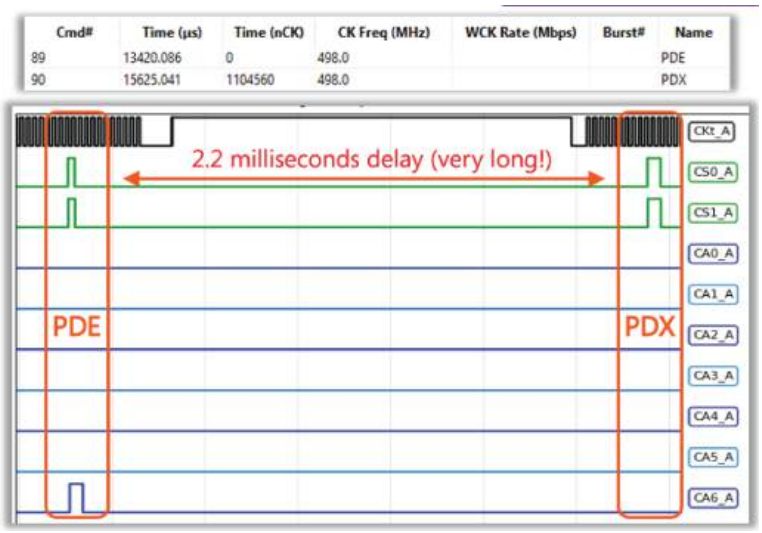


Instantaneous frequency is tracked as shown above.

Figure 9: Clock Change as Observed in the Logic Signals

Clock Stop Tolerance

The M7030 Analyzer tolerates prolonged clock stoppage during memory power-down or low-power operation. Because the analyzer is not synchronized to the controller clock, it can continue tracking capture context across clock-stop events and report the duration of the stoppage in the timestamp data.



Note that timestamps show how long the clock has stopped.

Figure 10: Long Clock Stoppage During Memory Power Down

Low-Power Debug Support

By supporting clock changes and clock stoppage, the analyzer is well suited for debugging modern DDR/LPDDR systems that use aggressive power-management states. Engineers can analyze protocol behavior before, during, and after low-power transitions without losing capture continuity.

CUSTOM TRIGGERS

Custom Trigger Definition

The M7030 Analyzer enables targeted live traffic capture using custom trigger conditions based on rank, Cycle0, and Cycle1 parameters. By matching the target memory rank and cycle-based command values, the analyzer can trigger acquisition on specific protocol conditions during memory-bus operation.

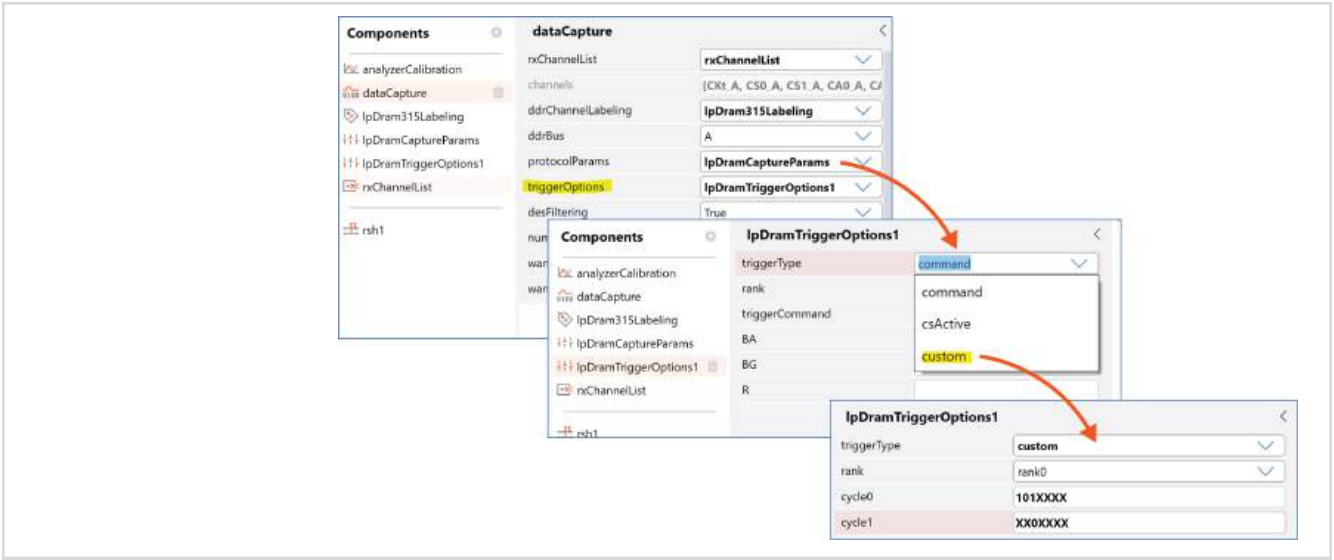


Figure 11: Custom Trigger Definition in the GUI

Specifications

This section describes the key electrical, performance, interface, triggering, environmental, and protocol capabilities of the M7030 Analyzer. Use these specifications to verify system compatibility, supported DUT signaling requirements, operating conditions, and protocol analysis capabilities before configuring or operating the hardware.

NOTE

Unless otherwise noted, all specifications apply under normal operating conditions. Specifications are subject to change without prior notice.

Table 1: General Specifications

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Application / Protocol			
Logic Capture	Arbitrary		The M7030 Analyzer can capture logic waveforms from any protocol as long as the signaling levels are within the receiver specifications.
Automatic Protocol Decode	DDR5 LPDDR5 LPDDR6		
Automatic Timing Analysis	DDR5 LPDDR5 LPDDR6		
Protocol-Based Triggering	DDR5 LPDDR5 LPDDR6		

Table 1: General Specifications (continued)

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Ports			
Number of Channels	36		Supports single-ended and differential signals under test.
Connections to PC for Pinetree Control	1		USB-C
Power and Environmental Conditions			
AC Input Voltage	120-240	V	
Maximum Power Dissipation	700	W	
Minimum Ambient Temperature	5	° C	
Maximum Ambient Temperature	35	° C	

Table 2: Sampling Rates and DUT Data Rates

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Maximum Sampling Rate	80	GS/s	
Minimum DUT Data Rate	80	Mbps	
Maximum DUT Data Rate	20,000	Mbps	
DUT Frequency Resolution	Arbitrary		The analyzer can track any frequency with a timing resolution of 12.5 ps.

Table 3: Receiver Characteristics

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Input Coupling			
Input Port Connection	DC Coupled		
Input Impedance	50	Ohm	
Voltage Specifications			
Minimum $\|V_{ID}\|$	90	mV	At the SMPM connector
Maximum $\|V_{ID}\|$	1400	mV	At the SMPM connector
Minimum Programmable Reference Voltage	0	mV	This is typically automatically trained in the analyzer. Software overrides exist for manually setting it.
Maximum Programmable Reference Voltage	1300	mV	This is typically automatically trained in the analyzer. Software overrides exist for manually setting it.
Timing Generator Performance			
Timing Resolution	0.78	ps	
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	Unlimited		

Table 4: Pattern and Protocol Features

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
General Pattern Architecture			
Total Memory Depth	24	Gbyte	
Memory Depth per Channel	667	Mbyte	Each channel gets an equal amount of storage.
Deselect Filtering	Available		Long durations of DES periods can be automatically filtered to save on pattern storage.
Capture Filtering	Available		The analyzer can be programmed to capture only certain types of commands, thus saving on pattern storage.
Protocol and Trigger Architecture			
Internal Trigger Conditions	Immediate Command Custom 1-Cycle Custom 2-Cycle		Based on DDR5, LPDDR5, and LPDDR6 protocols.
External Trigger Conditions	GPIO	2	Trigger Input/Flag Output

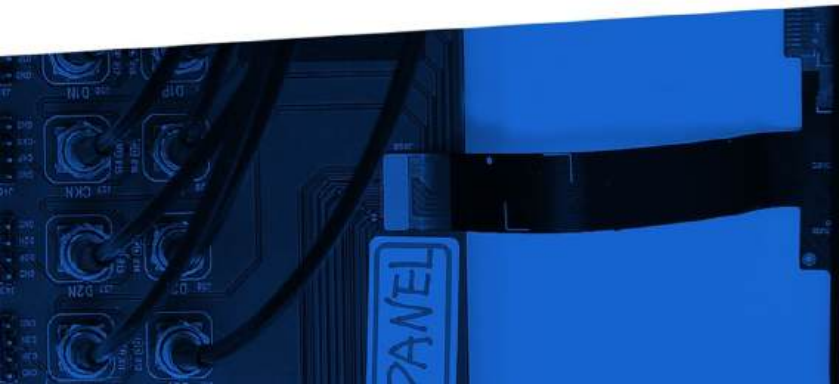
Table 5: Trigger and Flag Voltage Characteristics

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
Voltage			
Voltage Level	1.8	V	All GPIOs operate at 1.8 V LVCMOS
V_{IL} Minimum	-0.2	V	

Table 5: Trigger and Flag Voltage Characteristics (continued)

PARAMETER	VALUE	UNITS	DESCRIPTION AND CONDITIONS
V_{IL} Maximum	0.6	V	
V_{IHL} Minimum	1.2	V	
V_{IH} Maximum	2.0	V	
V_{OL} Maximum	0.45	V	
V_{OH} Maximum	1.35	V	

REVISION NUMBER	HISTORY	DATE
1.0	Document Release.	May 7, 2026
1.1	Minor edits to Pinetree section. Removed CSI-2 and MIPI references. Other formatting changes.	May 11, 2026



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